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Master's Thesis

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Power amplifier design and implementation for loosely coupled wireless power transfer system

Thesis supervisor: Prof. Raimo Sepponen
Thesis advisor: DI Pekko Ruippo

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Abstract

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The exploitation of magnetic resonance induction in wireless power transfer system where two magnetically coupled tuned resonators forms an energy transfer path is introduced. Starting from equivalent circuit of coupled LC-resonators the expression for maximum power transfer efficiency was derived and it was found that coupling factor and resonators Q values are determinant in power transfer efficiency.

Class D ZVS (zero voltage switching) and Class E switch mode power amplifiers were studied and prototype power stages were designed and implemented. Both amplifiers were tested with A4WP compliant coil set at 6.78MHz operation frequency. Several performance tests were carried out and at the end amplifier topologies were compared with respect to power transfer efficiency. According to the results both amplifier topologies met the high efficiency requirement needed in wireless power transfer, even though those both have their own optimal operation conditions where maximum efficiency is achieved. As a result topology selection table was presented as a tool for designer and design guidelines concerning amplifier topology selection, PWB layout, amplifier ZVS tuning and EMI were introduced.

Previously in RF engineering exclusively seen GaN FETs are breaking into area of power electronics and the interest in their excellent switching characteristics brought them also part of this work. Both amplifiers were implemented by using GaN FETs as a switching device and high performance were proved by thermal measurements and observing switching waveforms. Main characteristics of GaN FET were studied and some qualitative comparison with MOSFET introduced.

Key words: Wireless power transfer, Magnetic resonance induction, Coupled resonators, GaN FET, Class E, Class D, Zero voltage switching

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Tiivistelmä

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Magneettista resonanssi-induktiota hyödyntävässä langattomassa tehonsiirtojärjestelmässä kaksi heikosti toisiinsa kytkettyä resonaattoria muodostavat tehonsiirtotien. Lähtien liikkeelle kytkettyjen LC-resonaattorien piirikaaviosta johdetaan lauseke tehonsiirtohyötysuhteelle ja havaitaan kytkentäkertoimen ja resonaattoreiden Q-arvojen olevan määräääviä tekijöitä tehonsiirtohyötysuhteen arvossa.

Työssä suunnitellaan ja toteutetaan kytkemistekniikkaan perustuvat D ja E-luokan tehovahvistimet. Kumpikin vahvistin testataan A4WP standardin mukaisella lähetin-vastaanotin parilla 6,78 MHz toimintataajuudella. Useita suorituskyky mittauksia suoritetaan ja lopuksi vahvistin topologioiden hyötysuhde arvoja vertaillaan. Kummankin vahvistin topologian havaitaan täyttävän langattoman tehonsiirto järjestelmän korkeat hyötysuhde vaatimukset, vaikka vahvistimien optimaaliset toiminta olosuhteet eroavatkin toisistaan. Työ tarjoaa suunnittelijoille ohjeita oikean vahvistin topologian valinnassa, piirilevyn suunnittelussa, vahvistimien optimaalisesta virityksestä sekä EMI näkökohdista.

Aiemmin yksinomaan radiotekniikassa käytetyt GaN FET transistorit ovat alkaneet herättää kiinnostusta myös tehoelektroniikan puolella. GaN FET kytkinkomponenttien erinomaiset kytkentäominaisuudet toivat ne myös osaksi tätä työtä. Työn molemmat vahvistimet toteutettiin GaN FET kytkimillä ja niiden erinomainen suorituskyky vahvistettiin mittauksin.

Avainsanat: langaton tehonsiirto, magneettinen resonanssi-induktio, kytketyt resonaattorit, GaN FET, E-luokan vahvistin, D-luokan vahvistin

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To my family, I would like to give my appreciation for your patience in those moments when I needed to work at home and take my time to studies. You have been understanding and supportive for me in many ways during the last few years, thank you. Moreover, I cannot be thankful enough for financial support I have got from my parents over the past years and I respect that you have always been supporting me on my biggest decision in my life.

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Antti Nurmi

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Used symbols

Φ_B=magnetic flux	[Wb]
B = magnetic flux density	[T]
η = efficiency	[%]
k = coupling factor	
εmf = electromotive force	[V]
μ_0 = permeability of free space	$4\pi * 10^{-7} \frac{Vs}{Am}$
Q = charge	[C]
L = inductance	[H]
M = mutual inductance	[H]
C = capacitance	[F]
ω = angular frequency	$[\frac{rad}{s}]$
f = frequency	[Hz]
V = voltage	[V]
I = current	[A]
P = power	[W]
R = resistance	[Ω]
X = reactance	[Ω]
j = imaginary unit	
$Z = R + Xj$ = complex impedance	[Ω]

Used Shortages

A4WP	Alliance for wireless power
AC	alternating current
BOM	bill of materials
CMOS	complementary metal oxide semiconductor
CSI	common source inductance
DC	direct current
DSBGA	die size ball grid array
DTBC	device to be charged
DUT	device under test
2DEG	two dimensional electron gas
EMC	electromagnetic compatibility
EMI	electromagnetic interference
FET	field effect transistor
FOD	foreign object detection
FOM	figure of merit
GaN	gallium nitride semiconductor
IC	integrated circuit
IEC	International electro technical commission
ISM	industrial science and medical
LC	combination of inductor and capacitor
LC WPT	loosely coupled wireless power transfer
LDO	low dropout
LGA	land grid array
MOSFET	metal oxide semiconductor FET
PTU	power transmitter unit
PRU	power receiver unit
PMA	Power matter alliance
PWM	pulse width modulation
PWB	printed wire board
RCE	resonator coupling efficiency
RF	radio frequency
RX	receiver
TC WPT	tightly coupled Wireless power transfer
TTL	transistor – transistor logic
TX	transmitter
UVLO	under voltage lock out
WPC	Wireless power consortium
WPT	wireless power transfer
ZVS	zero voltage switching
ZCS	zero current switching

1 Introduction

Nowadays people have a large number of different portable devices that need to be charged regularly in dense cycle. Most of the people has come up to the challenge in storing variety of chargers and cables for different appliances feeling it frustrating and inconvenient. A smart phone is typical example of mobile device that need to be charged often mainly due to the underrated battery capacity. New fast charging appliances and USB Type-C connectors are giving some help in smartphone functionality, but still wires are needed.

Since 2011 there has been in markets electromagnetic induction based wireless charging docks for smart phones. Power is delivered through close together placed pair of transmitter and receiver coils while power transmission efficiency is strongly depended of coupling factor between coils. The requirement for tightly coupled coils leads to demand for precise coil alignment and close coil proximity. The consequence of exact device placement requirement over charging dock is challenging and inconvenience for the consumer.

At the moment there are large scale interest in consumer electronic industry to find solutions to improve consumer convenience with wireless charging. The most promising solution to extend the freedom of placement and convenience in wireless charging is the magnetic resonance induction, which was initially introduced by research group led by Marin Soljačić at MIT University Department of physics in 2007. Magnetic resonance induction makes possible to have great power transmission efficiency even in a case of loosely-coupled transmitter and receiver coils. A major step forward in user convenience would be wireless charging where same charging dock would suite for all appliances and simultaneous multi-device charging would be possible.

The starting point in this thesis work is to disclose the physical phenomenon behind electromagnetic induction and expand awareness of the exploitation of magnetic resonance induction in wireless power transfer. In magnetic resonance induction based wireless power transfer the tuned coupled LC-resonator pair is the fundamental building block and understanding its behaviour is accelerated with help of circuit analysis techniques. Moreover, expression for the maximum theoretical power transfer efficiency in magnetic resonance induction based wireless power transfer is derived. The results obtained in this work confirms the importance of high Q-value resonators that are needed to achieve high power transfer efficiency in magnetic resonance induction based wireless power transfer.

Both electromagnetic induction exploiting wireless power transfer principles have their own pros and cons that will be discussed shortly in the beginning of this composition. The focus in comparison is to point out what are the advantages of magnetic resonance induction based wireless power transfer in consumer point of view and justify the importance of continuation of the research and development.

Most of the technical challenges related to magnetic resonance induction WPT are originated from relatively high operation frequency. In electromagnetic induction based WPT systems operation frequencies are few hundred kilohertz whereas in magnetic resonance induction WPT operation frequency is chosen to be fixed 6.78MHz. Relatively High operation frequency makes power amplifier design challenging because efficiency requirement is same time high. To meet high efficient requirement only choice is to use switch mode power amplifier. In this work Class D and Class E switch

mode amplifiers are studied and prototype power stages are designed and implemented. Switching losses are proportional to switching frequency and thus soft-switching topologies are in interest of this work. Several performance test are carried out for amplifiers and at the end performance of both topologies are compared with respect to efficiency. The main object is to produce such information that can be used when suitable amplifier topology for commercial application is searched.

The introduction of higher operation frequency impose some new demands for switching device used in power stages of WPT systems. Higher switching frequency increases switching losses and that has disastrous effect on systems total energy efficiency. Previously in RF engineering exclusively seen GaN FETs are breaking into area of power electronics and the interest in their excellent switching characteristics brought them also part of this work. Main characteristics of GaN FET are studied here and some qualitative comparison with MOSFET are introduced.

High switching frequency and fast switching transitions are liable to constitute challenging EMI issues. During this work different electromagnetic interference coupling ways into electrical system are discussed and generic instructions are given how electromagnetic interference can be reduced. For sure EMI issues are big challenge in magnetic resonance induction based WPT system. Unfortunately this work do not give thorough solution how to pass official EMC test practices, but it offers some guidance and knowledge of critical EMI issues in design and PWB layout.

Vladimir A. Muratov, Texas Instruments:

"*User experience is the key factor that drives technology development, paving the way for safer and more convenient devices accompanying us in everyday life.*"

2 Wireless power transfer methods

Most of the WPT methods known are based on electromagnetics. As an exception could be mentioned ultrasonic or other method that employs some medium in power transfer path. In fig.1 WPT methods that relay on electromagnetics are divided in near field and far field in respect of wavelength of electromagnetic wave. The boundary between near field and far field (fig.2) is somewhat nebulous but roughly far field can be said to begin when distance d from source is much longer than the wavelength λ of electromagnetic wave $d >> 2\lambda$. In non-radiative near field we are certainly when $d < \frac{\lambda}{2\pi}$. [1]

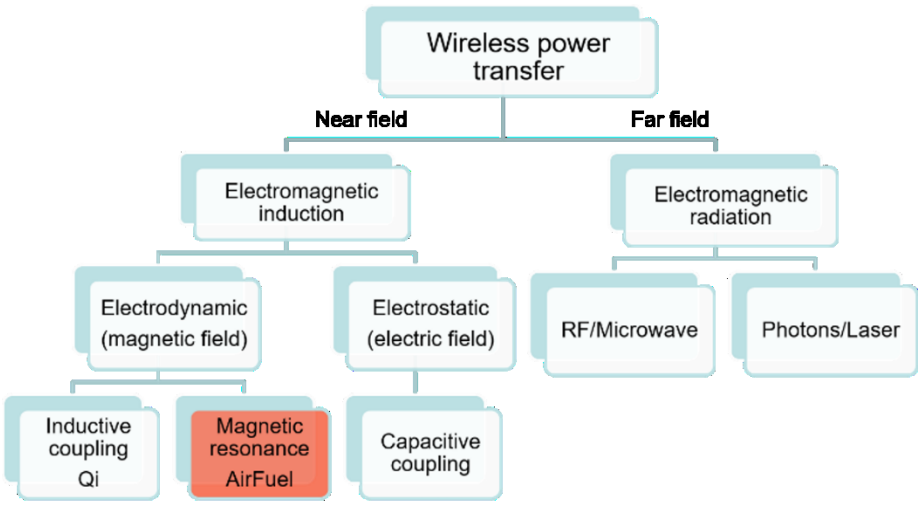

Figure 1 Different methods for wireless power transfer.

Interest of this work relays firmly on electrodynamic branch of WPT and more specify in magnetic resonance induction, where the distance between source and receiver coil is such that power transfer happens in non-radiative near field. In non-radiative region reactive energy is oscillating between source and reactive near field without losing energy, when receiver is placed close enough the source, reactive energy can be absorbed into receiver and power is transferred. Energy flow from source to receiver increases current in source coil and it is seen as an impedance shift by transmitter i.e. power amplifier.

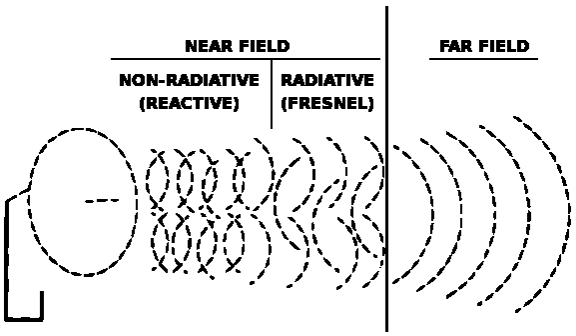

Figure 2 Near field and far field. Image source: https://en.wikipedia.org/wiki/Near_and_far_field.

Definition of loosely and tightly coupled WPT

Depending on the magnitude of coupling factor electromagnetic induction based wireless power transfer systems can be classified either loosely coupled or tightly coupled. Coupling factor k defines how large portion of primary coil magnetic flux is affecting in energy transportation between primary and secondary coil. In definition of coupling factor k L_1 and L_2 are self-inductances of coupled coils, M points out mutual inductance between coils. [2]

$$k = \frac{M}{\sqrt{L_1}\sqrt{L_2}}$$

Coupling factor may vary between 0 and 1. One means perfectly coupled situation when all flux generated by primary coil is penetrated through secondary coil. Coupling factor zero means that coils are independent of each other. When k > 0.5 coils are said to be tightly coupled, while k < 0.5 coils are said to be loosely coupled.

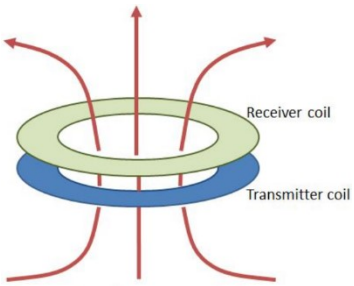

Figure 3 Tightly coupled transmitter and receiver coils. Image source: www.wirelesspowerconsortium.com

In fig. 3 there is tightly coupled pair of coils, same magnetic flux goes through both coils. Typically loose coupling in fig. 4 occurs while there is large distance between coils or coils are different size. Typically tightly coupled wireless power transfer system means purely inductive based approaches. Instead loosely coupled wireless power transfer system means usually exploitation of resonance-induction principle.

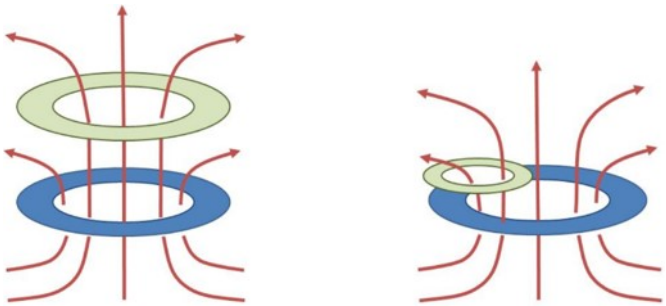

Figure 4 Two examples of loosely coupled coils. Image source: www.wirelesspowerconsortium.com

2.1 Tightly coupled electromagnetic induction based WPT

Tightly coupled wireless power transfer in fig. 5 relays purely on electromagnetic induction. Alternating current in supply side coil produces alternating magnetic field. Major part of magnetic flux from supply coil penetrates through power receiving coil and according to the Faraday's law of induction electromotive force is induced into receiver coil and fed to the load.

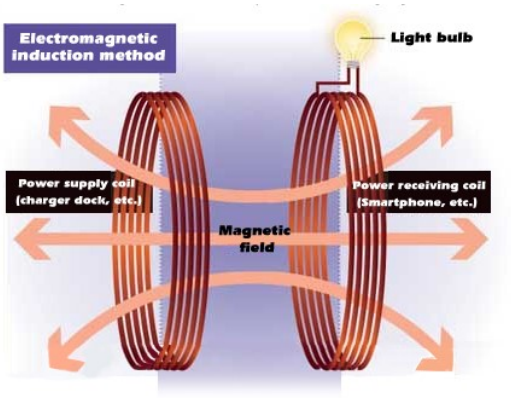

Figure 5 Tightly coupled electromagnetic induction based WPT. Image source: http://www.chinaipmagazine.com/en/upload/eWebEditor/2013112891610225.jpg

2.2 Loosely coupled magnetic resonance induction based WPT

The principle of magnetic resonance induction based WPT is shown in fig.6. Time-varying current in source resonator creates magnetic field that couples transmitter and receiver side together. Both resonators are tuned in same resonance frequency and small fraction of source coils magnetic flux is able excite resonance in device resonator and launch the energy build up. Loose coupling between resonators lead to that energy is fluctuating back and forth between coupled source and receiver, effectively there is resonance between source and receiver sides. High Q-value of source and receiver resonators maintain energy levels. When receiver is loaded, energy flows out of coupled resonator pair and new energy into resonating system is drawn from power supply.

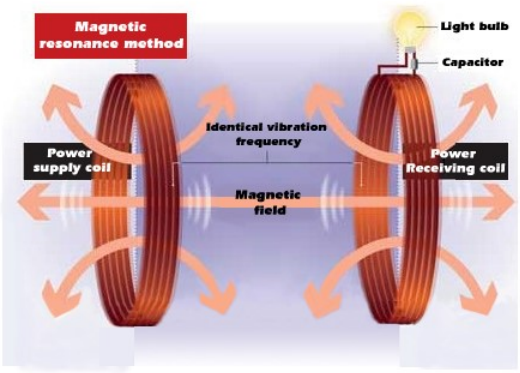

Figure 6 Coil coupling is loose in magnetic resonance induction method. Image source: http://www.chinaipmagazine.com/en/upload/eWebEditor/2013112891640206.jpg

2.3 Comparison of loosely and tightly coupled WPT methods

It is quite easy to find advantages of loosely coupled wireless power transfer in contrast tightly coupled alternative. In LC WPT coupling factor $k = 0{,}1$ or even smaller is often satisfactory and leads to the fact that source and receiver coils not need to be same size and very close to each other. Larger source coil provides broader charging area, more freedom in placement and makes simultaneous multi-device charging possible (fig.7 right). Larger separation between coils makes integration of power transmitter unit to the furniture, automotive environments etc. easy. Definitely the main advantage of LC WPT is the increased user convenience. Ideally same charging device is able to power all portable electronic devices needed that person needs. In tightly coupled wireless power transfer efficient power transfer is achieved only if source and receiver coils are very close to each other and concentrically positioned. In TC WPT source coil is able to deliver power only one receiver at a time (fig. 7 left). Usually coils are about same size in TC WPT which makes magnetic flux guiding and surrounding electric circuit shielding somewhat easier. Probably EMI handling in TC WPT is easier compared to the LC WPT.

While benefits and flexibility of LC WPT attracts customer side, most of the negative issues related to LC WPT need to be carried through by designer and developers. What is seen as increased convenience in customer side is seen as variable loading conditions in WPT system point of view. Variety of devices to be charged with the same charging unit and varying loading conditions causes load impedance shifts. Adaptive impedance matching is most probably needed between power amplifier and source coil to maintain efficient power transfer in all possible loading conditions. Advantage of TC WPT is that simpler power stage and matching circuit is needed. Tightly coupled coils ensures that there are not so much fluctuation in impedance seen by power amplifier.

Figure 7 Left: TC WPT image source: http://images.dailytech.com/nimage/SGS4Qi-9161.jpg Right: LC WPT Image source: http://wmpoweruser.com/wp-content/uploads/2014/01/image_thumb36.png

3 Theory of loosely coupled WPT

Magnetic coupled coil pair can be seen as fundamental subsystem in loosely coupled wireless power transmission. In the following chapter will be composed simplified model of series resonance tuned coupled coil set. Mutual inductance between coils determines strength of magnetic coupling.

3.1 Mutual inductance between coupled coils

In fig. 8 TX coil is located on x-y plane in the origin and RX coil is concentrically located at distance d above TX coil in z-axis. It is assumed that $r_1 \gg r_2$.

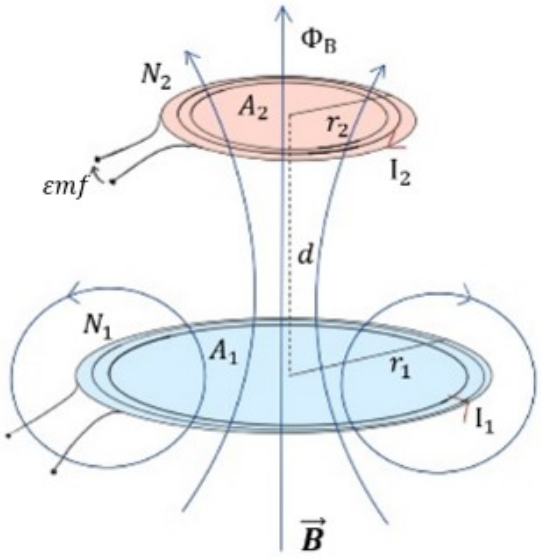

Figure 8 Electromagnetic induction between two adjacent coils.

In TX coil there is current I flowing which produces magnetic field around coil. In conductor each moving charged particle produces own minor magnetic field that are superpositioned as a total magnetic field of current carrying conductor. The law of Biot and Savart [3] defines differential magnetic flux density $\vec{\boldsymbol{B}}$ of differential current element of conductor (1). In (1) $Id\vec{\boldsymbol{l}}$ is infinitesimal current source in coil ring, $\hat{\mathrm{r}}$ is unit vector in the direction of the viewed field point and $\mu_0 = 4\pi * 10^{-7} \frac{Vs}{Am}$ is permeability of free space.

$$d\vec{\boldsymbol{B}} = \frac{\mu_0}{4\pi} * \frac{Id\vec{\boldsymbol{l}} \times \hat{\mathrm{r}}}{\mathrm{r}^2}. \tag{1}$$

By integrating over all current segments $d\boldsymbol{l}$ the total magnetic flux density at any point in space can be calculated:

$$\vec{\boldsymbol{B}} = \frac{\mu_0}{4\pi} \int \frac{Id\vec{\boldsymbol{l}} \times \hat{\mathrm{r}}}{\mathrm{r}^2} \tag{2}$$

Biot-Savart law can be used to derive following expression for circular coil magnetic flux density on the z-axis above coil.

$$B_z(z) = \frac{\mu_0 I_1 r_1^2 N_1}{2(r_1^2+z^2)^{\frac{3}{2}}} \tag{3}$$

Next we define the magnetic flux Φ_M through a surface. Differential magnetic flux is

$$d\Phi_{\mathrm{B}} = \vec{\boldsymbol{B}} \cdot d\vec{A} \tag{4}$$

The total magnetic flux Φ_M is then integral over surface

$$\Phi_{\mathrm{B}} = \int \vec{\boldsymbol{B}} \cdot d\vec{A}\,. \tag{5}$$

Referring to the initial assumptions the magnetic flux density may be considered uniform over the area of RX coil. Thus, we get [3] for magnetic flux through RX coil at distance $z = d$ from TX coil.

$$\Phi_{\mathrm{B}} = B_Z(d)A_2 = \frac{\mu_0 i_1 N_1 \pi r_1^2 r_2^2}{2(r_1^2+\mathrm{d}^2)^{\frac{3}{2}}} \tag{6}$$

Faraday's law [3] of induction says that electromotive force εmf is equal to time derivative of magnetic flux Φ_B through the closed conducting wire loop. Negative sign can determined by Lenz's law [3], which says that the direction of any effect caused by magnetic induction is opposed to the original cause of the effect. In expression (7) is substituted alternative current $I_1 = i_1$.

$$\varepsilon mf = -\mathrm{N}_2 \frac{d\Phi_B}{dt} = -N_2 \frac{d}{dt}(B_z(z)A_2) = -N_2 \frac{d}{dt}\left(\frac{\mu_0 i_1 N_1 \pi r_1^2 r_2^2}{2(r_1^2+\mathrm{d}^2)^{\frac{3}{2}}}\right) \tag{7}$$

Interaction between TX and RX coils can be characterized also by mutual inductance M. Mutual inductance between two adjacent coils is defined in terms of average magnetic flux Φ_B through coil 2 caused by the current in coil 1. Mutual inductance is always reciprocal phenomenon. If coils are wounded from several turns N_1 and N_2, they become multiplication factors to the equation. [3]

$$M = \frac{N_2\Phi_{B2}}{i_1} = \frac{N_1\Phi_{B1}}{i_2}. \tag{8}$$

From definition of mutual inductance (8) it can be written

$$Mi_1 = N_2\Phi_{B2}$$

$$M\frac{di_1}{dt} = -\mathrm{N}_2 \frac{d\Phi_{B2}}{dt} \tag{9}$$

Now by combining (7) and (9) it can be written

$$M\frac{di_1}{dt} = -N_2 \frac{d}{dt}\left(\frac{\mu_0 i_1 N_1 \pi r_1^2 r_2^2}{2(r_1^2+\mathrm{d}^2)^{\frac{3}{2}}}\right) \tag{10}$$

Now it is shown that, mutual inductance M between two adjacent concentric circular coils on the same axis depends on coil areas, distance between coils, number of turns in coils and the permeability of medium between coils. Assumption here is that $r_1 \gg r_2$.

3.2 Equivalent circuit model of coupled resonators

Based on circuit model of coupled source and device resonators in fig.9, expression for power transfer efficiency is derived. Further developing, optimal load resistance $R_{load,opt}$ and expression for maximum power transfer efficiency η_{max} is found. At the end simple relation of coupling factor k and resonator individual quality factors $Q_{s,d}$ to the power transfer efficiency is introduced. Similar results are shown by [4] [5]. In last part input impedance Z_{in} seen by power amplifier dependence on mutual inductance M and load resistance R_{load} variations is demostrated. In fig. 9 V_S is voltage source, $R_{s,d}$ are coil resistances, $L_{s,d}$ are coil inductances, $C_{s,d}$ are series resonance capacitors, M is mutual inductance and R_{load} refers to load resistance. The T-transformation for circuit in fig. 9 simplifies derivation and it is shown in fig. 10

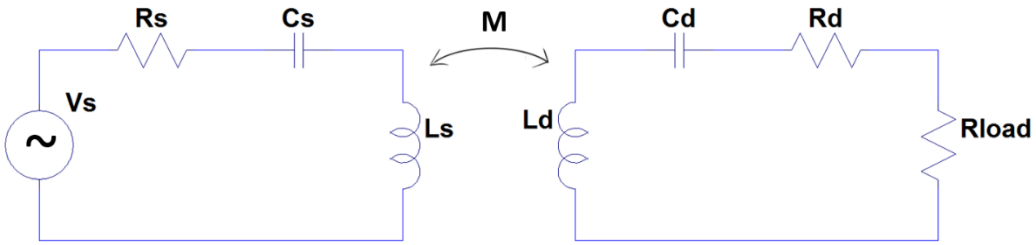

Figure 9 Equivalent circuit for coil set in magnetic resonance induction based WPT.

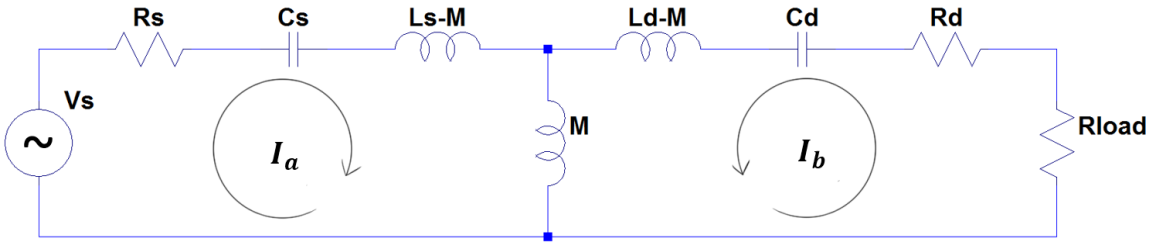

Figure 10 Equivalent circuit after T-transformation.

Equations for loop currents I_a and I_b in fig.10:

$$\left(R_s + \frac{1}{j\omega C_s} + j\omega L_s - j\omega M + j\omega M\right) I_a + j\omega M I_b = V_s$$
$$(R_{load} + R_d + \frac{1}{j\omega C_d} + j\omega L_d - j\omega M + j\omega M) I_b + j\omega M I_a = 0$$

$$\left[R_s + \left(\omega L_s - \frac{1}{\omega C_s}\right) j\right] I_a + j\omega M I_b = V_s$$
$$\left[(R_{load} + R_d) + \left(\omega L_d - \frac{1}{\omega C_d}\right) j\right] I_b + j\omega M I_a = 0$$

Ideally in resonance $\omega = \omega_0$. Expressions $\left(\omega L_s - \frac{1}{\omega C_s}\right)$ and $\left(\omega L_d - \frac{1}{\omega C_d}\right)$ in current equations

become equal to zero and equations for loop currents I_a and I_b simplifies:

$$R_s I_a + j\omega_0 M I_b = V_s \tag{11}$$

$$(R_{load} + R_d) I_b + j\omega_0 M I_a = 0 \tag{12}$$

From above equatios (11) and (12) loop currents I_a and I_b can be solved as follows:

$$I_a = \frac{V_s(R_{load} + R_d)}{R_s(R_{load} + R_d) + \omega_0^2 M^2}$$

$$I_b = -\frac{V_s j\omega_0 M}{R_s(R_{load} + R_d) + \omega_0^2 M^2}$$

To calculate the power transmission efficiency η power delivered to source coil and power delivered to R_{load} are defined.

$$P_s = V_s I_a = \frac{V_s^2(R_{load} + R_d)}{R_s(R_{load} + R_d) + \omega_0^2 M^2}$$

$$P_{load} = R_{load}|I_b|^2 = \frac{R_{load} V_s^2 \omega_0^2 M^2}{(R_s(R_{load} + R_d) + \omega_0^2 M^2)^2}$$

The power transmission efficiency η:

$$\eta = \frac{P_{load}}{P_s} = \frac{R_{load} V_s^2 \omega_0^2 M^2}{(R_s(R_{load} + R_d) + \omega_0^2 M^2)^2} * \frac{R_s(R_{load} + R_d) + \omega_0^2 M^2}{V_s^2(R_{load} + R_d)}$$

$$\eta = \frac{R_{load}\omega_0^2 M^2}{(R_{load}+R_d)\left(R_s(R_{load}+R_d)+\omega_0^2 M^2\right)} \tag{13}$$

Above equation shows that at resonance power transmission efficiency depends on coil resistances R_s and R_d, load resistance R_{load}, mutual inductance M and resonant frequency ω_0. Same kind of results are shown by [4]. Earlier it was shown that mutual inductance depends only on geometric variables of coil set. By taking partial derivative from power transmission efficiency η with respect to R_{load} and setting it zero, optimal load resistance $R_{load,opt}$ can be found.

$$R_{load,opt} = R_d * \sqrt{1 + \frac{(\omega_0^2 * M^2)}{R_s R_d}} \tag{14}$$

By substituting (14) into (13) we get

$$\eta_{max} = \frac{\sqrt{1+\frac{(\omega_0^2 * M^2)}{R_s R_d}} - 1}{\sqrt{1+\frac{(\omega_0^2 * M^2)}{R_s R_d}} + 1} \tag{15}$$

Grajski [4] defines mutual quality factor $Q_M = \frac{\omega_0 M}{\sqrt{R_s R_d}}$. (16)

By substituting (16) into (15) we get

$$\eta_{max} = \frac{\sqrt{1+Q_M^2}-1}{\sqrt{1+Q_M^2}+1} \quad (17)$$

$$Q_M = \frac{\omega_0 M}{\sqrt{R_s R_d}} = \frac{\omega_0 k\sqrt{L_s L_d}}{\sqrt{R_s R_d}} = k\sqrt{Q_s Q_d} \quad (18)$$

In expression (18) $Q_{s,d} = \frac{\omega_0 L_{s,d}}{R_{s,d}}$ are source and device coil individual unloaded quality factors. Couplin factor definition was used in expression (18), $k = \frac{M}{\sqrt{L_s L_d}}$.

The mutual quality factor $k\sqrt{Q_s Q_d}$ can be defined as System figure-of-merit FOM [5]. In fig. 11 below is plotted maximum efficiency in function of mutual quality factor Q_M. Expression for mutual quality factor Q_M and plot in fig.11 proves that it is possible to get very high power transfer efficiency even with low couplin factor values as long as individual coil quality factors Q_s and Q_d are high. For example coupling factor $k = 0{,}1$ and individual quality factors $Q_s = Q_d = 200$ gives mutual quality factor $Q_M = k\sqrt{Q_s Q_d} = 20$ leading to maximum power transfer efficiency value 90% as in fig. 11 can be seen . Quality factor $Q = 200$ for individual PWB coil is not exceptionally difficult to achieve.

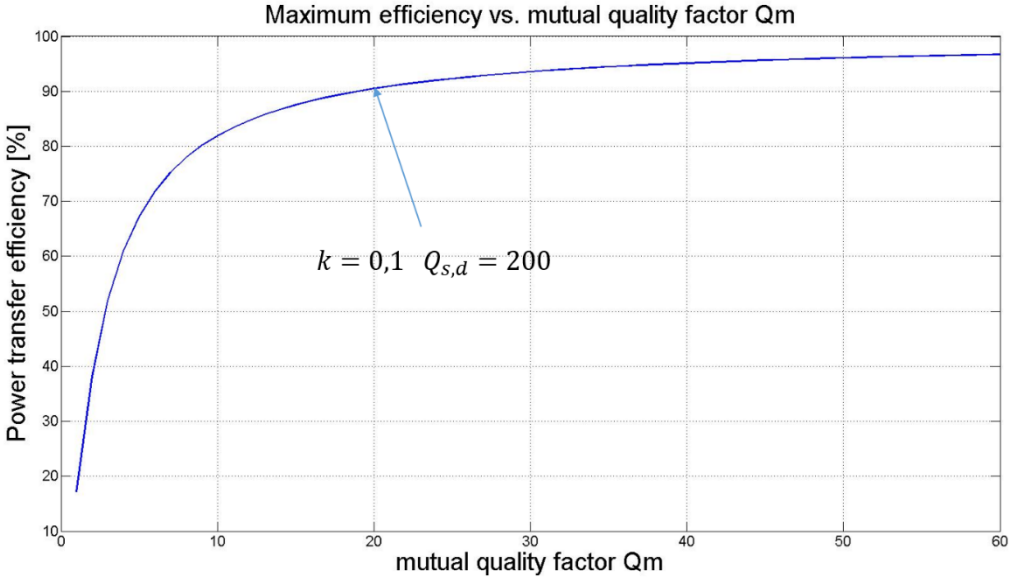

Figure 11 Maximum power transfer efficiency.

The input impedance Z_{in} seen by power amplifier:

$$Z_{in} = \frac{V_s}{I_a} = \frac{V_s}{\frac{V_s(R_{load}+R_d)}{R_s(R_{load}+R_d)+\omega_0^2 M^2}} = R_s + \frac{\omega_0^2 M^2}{(R_{load}+R_d)} = R_s + \frac{\omega_0^2 k^2 L_s L_d}{(R_{load}+R_d)} \quad (19)$$

From equation (19) it is obvious that the input impedance Z_{in} seen by power amplifier depends on mutual inductance M between source and device coil and load resistance R_{load} variations when both coils are in resonance. Plot in fig.12 shows natural charectresitic of coupled coil set, increasing the secondary side load resistance decreases the coil set total input impedance seen in primary side coil input. In plot coil resistances $R_{s,d} = 100m\Omega$, resonant frequency $\omega_0 = 2\pi * 6{,}78MHz$ and $L_{s,d} = 1{,}5\mu H$ values were used. Mutual inductance variation in fig.12 is modelled with variation of coupling factor k, which is more intuitive presentation of mutual inductance.

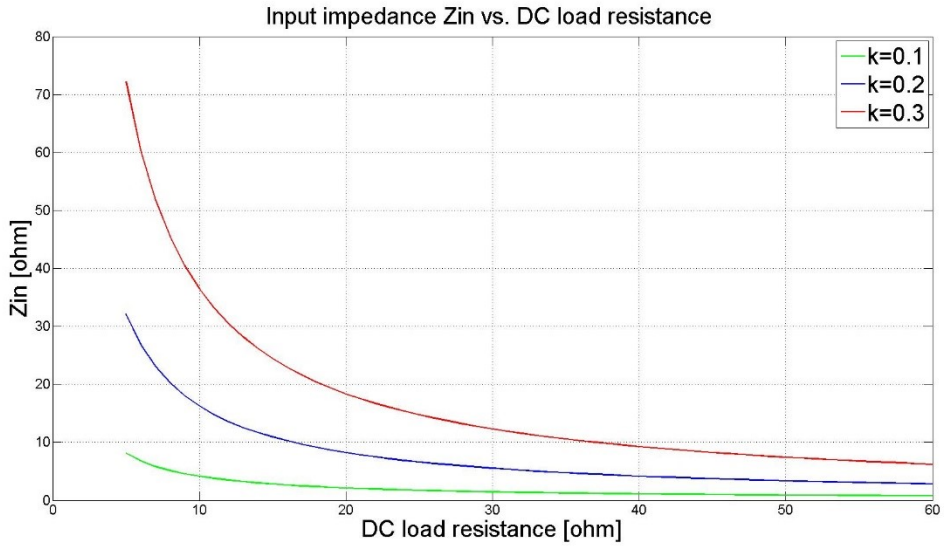

Figure 12 Input impedance dependence on coupling factor and DC load resistance.

The input impedance Z_{in} dependence on coupling between coils and load resistance R_{load} variations is important, because it affects the matching between power amplifier and coil set. If power amplifier output impedance is $Z_{PA,out}$, the maximum power is delivered from power amplifier into load when $Z_{in} = Z_{PA,out}^{*}$ i.e. conjugate matching [6].

4 Design considerations in LC WPT

At the moment there are two known approaches in wireless power transfer, the better known and widely adopted electromagnetic induction based Qi™ and still rarely seen magnetic resonance induction based AirFuel™. Qi™ is creation of Wireless Power Consortium (WPC), which was founded in 2008 by group of companies dealing with consumer electronics. First smartphones using Qi™ wireless technology were announced in 2011. While Qi™ is experienced and widely approved, AirFuel™ can be said to be a newcomer in wireless power transfer business. New AirFuel™ Alliance was launched in November 2015 and it is constituted on the basis of A4WP Rezence wireless charging platform. In the new AirFuel™ Alliance have former A4WP (Alliance for wireless power) and PMA (Power matter alliance) joined their forces to make more respectable contender in field of wireless power transfer.
In early 2016 the AirFuel™ Alliance will have their A4WP standard in IEC voting to be approved as an official wireless charging standard. As this work deals with magnetic resonance induction based WPT A4WP standard and related design challenges are introduced.

4.1 A4WP standard proposal

The operating frequency of A4WP WPT system is fixed 6.78 MHz, which belongs to lowest ISM frequency band. The standard defines six PTU classes in 2 – 70W power range and seven PRU gategories in 3.5 – 50 W power range. The bi-directional Bluetooth link between PTU and PRU is used to power control, to load identification and protection. The A4WP defines load impedance range and efficiency requirements for all six PTU classes. While PTUs are strictly specified standard allows flexible PRU design. A4WP compliant WPT system can transfer power from one PTU to one or more devices at the same time fig.13. [7]

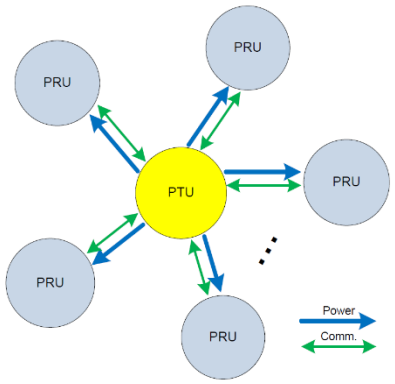

Figure 13 Basic architecture of A4WP WPT system. [7]

Fig. 14 gives an argument for 6.78MHz switching frequency. Increasing the operation frequency increases coil Q-value until the point where radiative losses begin to limit the maximum Q-value is reached. Maximal Q-value is achieved in intersection of coil resistive losses related Q_{abs} and coil radiation losses related Q_{rad}. Power transfer is based on magnetic resonance induction between two loosely coupled LC-resonators. Resonator Q-values need to be high in order to achieve high power transfer efficiency. Other advantage in selected 6.78MHz switching frequency is that minor foreign metal objects heating is seen on that frequency [8].

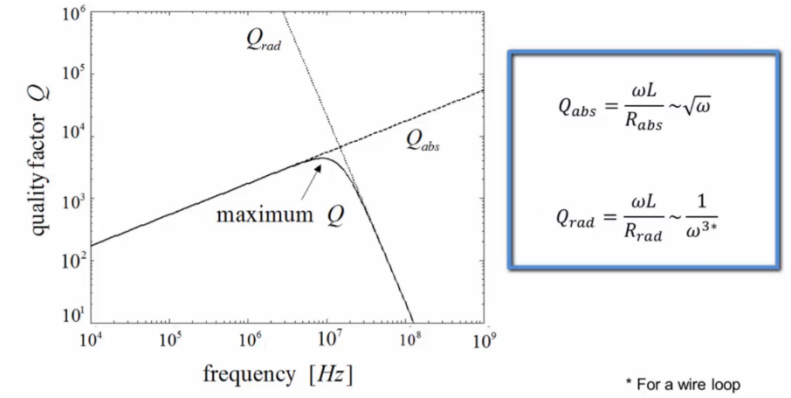

Figure 14 Argument for 6.78MHz operation frequency. Image source: www.WiTricity.com

Fig. 15 shows block diagram of A4WP wireless power transfer system. Source side of system consists of needed power electronics to convert AC-mains to proper DC level. High frequency switching mode amplifier generates pulsed current flow which is fed through impedance matching network to the source resonator. Typically a rectifier circuit needed to convert AC power into DC before load. PTU and PRU devices can communicate via bi-directional Bluetooth connection. [7]

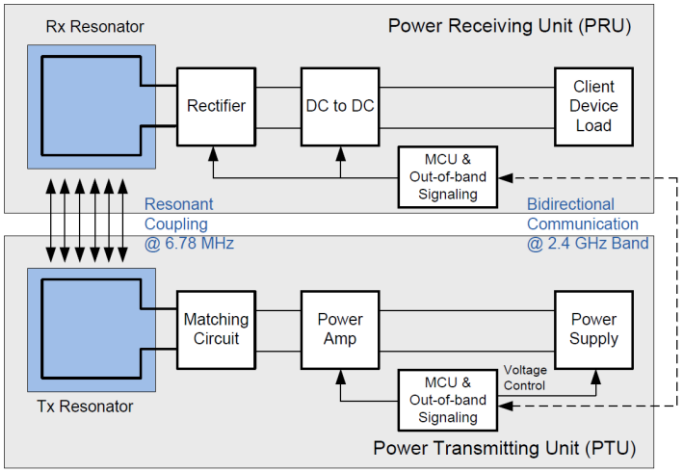

Figure 15 A4WP WPT system block diagram. [7]

4.2 GaN FET vs. MOSFET

The introduction of relatively high operation frequency of A4WP imposes new demands for switching devise used in power amplifier. Higher switching frequency increases switching losses and that may have disastrous effect on systems efficiency. Lately there have been seen great interest in gallium-nitride (GaN) based power FETs. Formerly these high electron mobility devices were used solely in RF engineering and known as HEMT. Now GaN FETs are introduced as an advantageous alternative for traditional Si based power MOSFETs and they are loaded with high expectations in power electronics. Fundamental operation and driving principles of both GaN FET and MOSFET are very close to each other, even though their internal structure and features differ significantly from each other. Later there will be seen design guidelines for GaN FET concerning layout, thermal performance and EMI.

Most of the superior features of GaN FET comes from the wide band gap semiconductor material. Wide band gap material ensures high resistant of electric field which means same time high breakdown voltage, ten times higher than Si have. Physical structures of actual components can be made smaller and more compact design can be used in integration. Smaller physical dimension and compact structure leads to small parasitic capacitances inside the component. Optimization of component package outfit also leads small parasitic inductances and makes fast switching possible. [9]

For silicon band gap energy is 1.1 eV, gallium arsenide 1.4eV. Wide band gap refers to energy levels of 3 eV or more. GaN has band gap 3.4 eV. Width of the band gap is related to atom size, lattice structure and bonding between atoms. Band gap energy refers to energy needed for particle to move valence band to the conduction band fig.16. For insulators band gap is very wide and for good conductor bang gap is narrow.

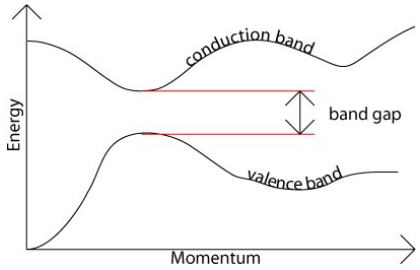

Figure 16 Energy band gap defines material conducting behavior. Image source: https://en.wikipedia.org/wiki/Wide-bandgap_semiconductor

Usually the higher electron mobility means better performance of semiconductor device. For GaN semiconductor material electron mobility is however fairly low when to compared Si. As an example of very high mobility semiconductor GaAs is mentioned here. Electron mobility @300K:

GaN: 900 $\frac{cm^2}{Vs}$ Si: 1500 $\frac{cm^2}{Vs}$ GaAs: 7500 $\frac{cm^2}{Vs}$

Fig.17 shows basic structure of GaN FET. Thin AlGaN layer on the top of GaN layer together forms a two dimensional electron gas channel 2DEG, where GaN semiconductor characteristic crystal lattice forms intrinsic piezo electricity which is employed with strain caused by AlGaN and GaN interface. 2DEG channel has much higher electron mobility than in a semiconductor material itself even as high as $2000\ \mu\frac{cm^2}{Vs}$ electron mobility is possible. The two dimensional electron gas explains the low R_{dson} of GaN FET. [10]

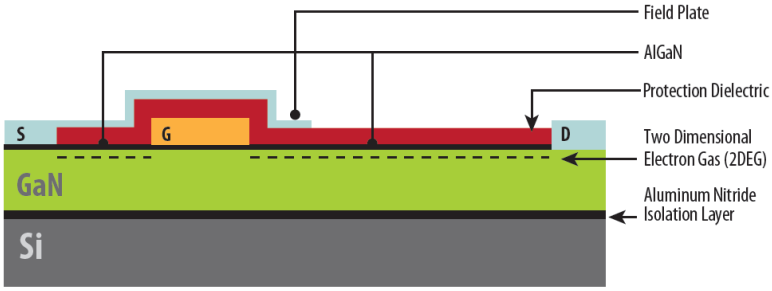

Figure 17 GaN FET structure. Image source www.epc/co.com

Gate charge Q_G is typically small in GaN FET, mainly due to its lateral construction (fig.18). Switching times for GaN can be 1ns while comparable break down voltage Si MOSFET switching time is about 6ns. Shorter switching times in addition to low R_{dson} reduce effectively losses in GaN FET.

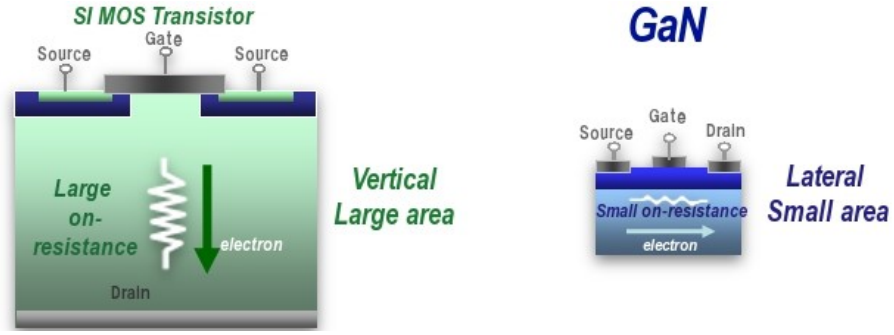

Figure 18 MOSFET vertical structure vs. GaN FET lateral structure. Image source: http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/

GaN FET does not contain intrinsic body-diode due to its lateral structure, however it has similar reverse conduction ability like silicon MOSFET. It is possible to turn on 2DEG layer of GaN FET in both directions. If gate-to-drain voltage V_{GD} is set to be higher than gate threshold voltage device start to conduct in reverse direction, with equal channel resistance $R_{DS_{on}}$ as in opposite direction. In fig.19 there is GaN FET schematic symbol, even though in the official schematic symbol there is body diode drawn it does not actually exist in real component.

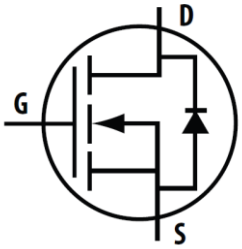

Figure 19 GaN FET circuit schematic symbol.

In MOSFETs there are pure PN-junction between drain and source which involves diode function. Characteristic for all diodes is the occurrence reverse recovery current I_{rr} when diode's forward polarity is changed and current is quickly turned to zero. The reverse recovery current I_{rr} is consequence of charge carriers, holes and electrons, accumulation back to their p- and n-regions making it possible to arise depletion zone between them. During the reverse recovery period there is a time when voltage and current exists simultaneously in diode resulting in switching losses within the diode. The same phenomenon in MOSFETS body diode increases turn-on losses of the device. The reverse recovery characteristic of the body diode is typically given as Q_{rr} reverse recovery charge and time t_{rr} in the datasheet. [11]

The absence of the body diode on GaN FET lead to that there is zero Q_{rr} reverse recovery charge and obviously no switching losses for that reason. Drawback of the absence of body diode is higher source-drain forward voltage during reverse conducting mode. In power conversion module, like half bridge, reverse current in switching devices occur typically during time interval when both devices are turned-off. GaN FET causes higher losses during dead time because its $V_{SD} \approx 2V$, double to comparable MOSFET $V_{SD} \approx 1V$.

Condition for GaN FET reverse conduction is $V_{GD} > V_{th}$.

Because $V_{GD} = V_{GS} + V_{SD}$, we get condition for source-drain forward voltage

$$V_{SD} > V_{th} - V_{GS}.$$

The above expression shows that negative V_{GS} voltage will increase the source-drain forward voltage drop over device and hence also reverse conduction losses are increased.

Demands for driver circuit

Even though, MOSFET and GaN FET driving is very similar in principle some special requirements are needed when operating with GaN FET. Here is discussion about special requirements for GaN FET driver circuits and differences compared to the similar MOSFET driving circuit. Lidow [9] states the three most important parameters for GaN FETs when considering gate driver requirements:

1) the maximum gate-to-source voltage $V_{GS,max}$
2) the gate threshold voltage V_{th}
3) the reverse conducting voltage drop V_F.

For GaN FET maximum allowable gate-to-source voltage $V_{GS,max}$ is significantly lower than corresponding silicon device. When $V_{GS,max}$ of GaN FET is +6V/-5V similar silicon MOSFET can resist +20/-20V gate-to-source voltages. The low $V_{GS,max}$ value is explained by thin AlGaN layer between gate and conducting 2DEG channel.

Also the gate threshold voltage V_{th} is typically lower for GaN FET. Fortunately, temperature coefficient for GaN FET's gate threshold voltage is much lower than MOSFET's. When 100℃ temperature rise for MOSFET can mean 30% lower V_{th}value, with same temperature transition GaN FETs V_{th} can be only 3% lower. [9]

Because of low V_{th} value of GaN FET and high di/dt and du/dt values due to fast switching, special concern in the driver circuit need to be given to prevent risk of Miller turn-on. Miller turn-on is possible incident e.g. in the half bridge topology in certain conditions. While high side switch is turned on, lower side switch faces high voltage change rate of du/dt across drain-to-source. Fast voltage change creates a current $i_{DG} = C_{DG}\frac{du}{dt}$ into parasitic Miller capacitor between drain and gate. Fig.20 demonstrates how one part of the current i_{DG} flows through the gate driver circuit into the ground while other part goes through C_{GS}. Depending on how large resistance current sees on the gate driver circuit path that higher voltage spike is produced into the gate. In some conditions there might be voltage over the V_T threshold in the gate and lower side switch is turned on unintentionally causing shoot-through, meaning that both switches are conducting in the same time. Shoot-through reduces efficiency dramatically and it is possible that severe damages are caused to the switching devices or other part of circuit. Lidow [17] gives the requirement for avoiding Miller-turn on:

$$C_{GD} * \frac{du}{dt} * (R_G + R_{sink}) * (1 - e^{-\frac{dt}{\alpha}}) < V_{TH}$$

Where dt is du/dt switching time that is in normal operation same as voltage rise time of switching device. In above equation α is the time constant $(R_G + R_{SINK}) * (C_{GD} + C_{GC})$. If switching times are needed to keep high to avoid losses, the best way to minimize risk of Miller turn of is to keep resistance $(R_G + R_{SINK})$ low in the gate circuit. To make it safe, it is recommend to keep gate drive pull-down resistance as low

as 0.5Ω or below that [17]. Miller capacitance Q_{GD} increases proportionally to the V_{DS}. Device with good Miller ratio given by [17]: $\frac{Q_{GD}}{Q_{GS}} * V_{TH} < 1$

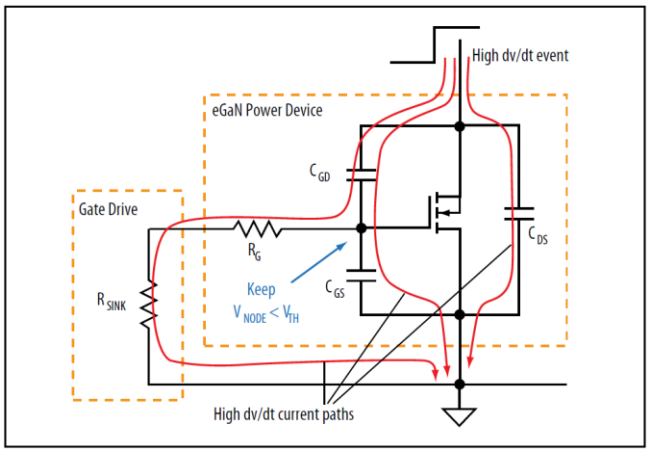

Figure 20 Miller turn-on current path. [9]

Even though fast switching times are desirable when trying to minimize switching losses, there might be several reasons to limit the speed of voltage transitions in switching device. As already mentioned too high du/dt can cause harmful shoot-through especially in hard switching topologies. Other reasons to restrict fast rise times are adjusting the switch node overshoot and ringing. High overshooting add voltage stress over switching device and along with ringing it can degenerate EMI performance. By flattening the edges of voltage pulse, meaning the high order harmonic frequency content are cut off. Resonances, caused by small parasitic capacitances and inductances in the circuit, are usually at very high frequencies and they can be restricted by limiting rise times.

To achieve optimal gate driving, pull-up and pull-down resistors should be adjusted separately. With power MOSFETS this is done typically by connecting diode and other resistor in parallel with gate resistor. Lidow [9] do not recommend this solution for GaN FETs due to their low gate threshold voltage. Instead of that they bring out idea of gate driver where pull-up and pull-down connections are separated to make it possible to adjust both current paths individually. Later is introduced Texas Instrument LM5113 gate driver [12], where this kind of solution is utilized.

As already has been discussed the absence of body diode in GaN FET and the higher voltage drop over GaN FET during reverse conducting (‘body diode’ operation) can lead into significant losses. Best way to reduce reverse conducting losses is to keep tight dead-time control. Shorter dead-times between switching means shorter reverse conducting intervals and less losses. How tight dead-time can be adjusted depends on switching time length and time variation. Features of GaN FET allows very tight dead-time control and definitely it is the thing that should be utilized when trying to achieve high efficiency levels.

Both switching device types benefit from parallel source-to-drain added schottky diode. Lower forward voltage drop across schottky causes lower diode conducting losses in both cases. Adding an external low inductance package schottky diode in parallel with GaN FET is possible if same time GaN FET has low parasitic package inductances and layout design enables to put components in close proximity. In most cases MOSFETs package inductances prevents using the external schottky diode, a monolithic integrated schottky is needed with MOSFET. [13]

Drawback of external schottky diode is increased output capacitance losses, but by optimal choose of schottky diode overall losses are decreased. Strydom & Reuch [13] founded that even 40% reduction in diode conduction losses can be achieved by adding external schottky diode in parallel to the synchronous rectifier (low side FET) in buck regulator. In practical terms decreased diode conduction losses gives wider effective dead-time range, it is easier to handle component tolerance and load variation influence in diode conducting losses if dead-time do not need to be as short as it would be without external schottky diode.

Thermal considerations

In order to achieve the maximum power density, the outline of GaN FET is minimized. Drawback of smaller outline is higher thermal resistance$R_{\theta JA}$, because heat emitting surface is smaller. In most cases, consumer electronics are designed to work without bulky and expensive heat sinks. Then most of the excess heat is conducted on the printed wire board. Table 1 below shows thermal conductivities of here relevant materials. Copper has distinctly highest thermal conductivity, which explains why PWB can be used effectively to transfer heat out of the components. PWB thermal performance depends on:

1) copper area in layout
2) copper thickness
3) PWB substrate material
4) airflow over the device.

The air has low thermal conductivity and natural air convection does not transfer heat effectively. Mechanically increased airflow improves significantly also component upper side thermal performance. Unfortunately, in most cases closed device housings are not supporting effective airflow. Thermal conductivities of some substantive materials in Table 1.

Table 1 Thermal conductivities.

Material	Air	Aluminum	Copper	GaN (thin film)	Si
$\kappa \quad [\frac{W}{mK}]$	0,024	215	400	200	130

By adding heat sink on the topside of GaN FETs cooling can be improved substantially. The thermal resistance $R_{\theta JA}$ of switching device reduces, because the area of heat transferring surface increases. If same heat sink is used to cover two or more GaN FETs it is recommended to use some thermally conducting and electrically insulating mouldable material between heat sink and components. Unevenly mounted, with different height or slightly tilted GaN FETs are fragile under pressure because of uncovered Si die material. Often GaN FETs substrate is connected to source and therefore electrical insulation is needed between GaN FET and heat sink, see fig.21.

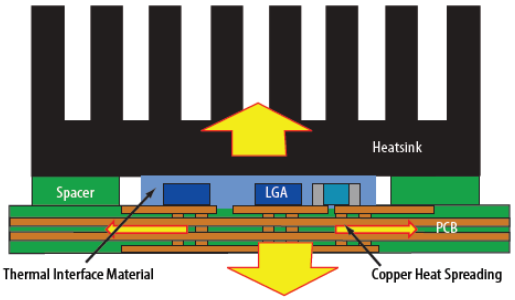

Figure 21 Heat sink assembling for LGA package GaN FET. Image source: www.epc-co.com

Some manufacturer uses in their product wafer level land grid array package (fig.22) that offers small inductance connections to the PWB and also heat transfer is effective in the direction of PWB.

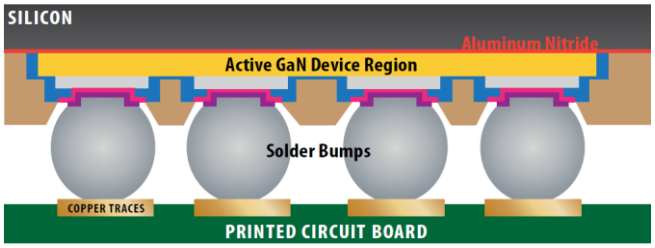

Figure 22 GaN FET flip-chip LGA package. Image source: www.epc-co.com

4.3 PWB layout considerations

Gate drive loop inductance

All the PWB traces can be thought as a transmission line that have such parasitic elements shown in fig. 23. Size of these parasitic elements are dependent of length, width and spacing between traces. In high operating frequencies these parasitic elements can cause resonating that can be seen as distortion in waveforms in output or as radiated EMI. Thought here used 6.78MHz is not in itself particularly very high frequency, all the harmonics that comes from edges of square wave are potential trouble makers.

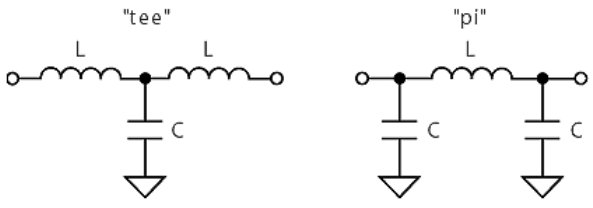

Figure 23 Lumbed element equivalents of a transmission line. Image source: http://mwrf.com/site-files/mwrf.com/files/archive/mwrf.com/Files/30/5541/Figure_01.gif

Next here is shown important layout consideration related to parasitic inductance between driver and switching device. Fig. 24 gives a simple precept to minimize the inductance in gate drive loop.

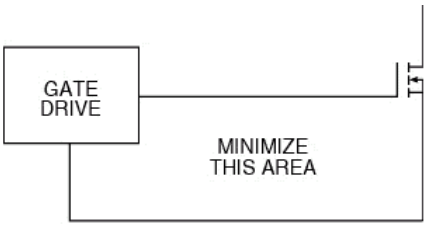

Figure 24 Simple rule to keep gate drive loop inductance small. Image source: http://www.planetanalog.com/document.asp?doc_id=527285

Gate drive loop inductance is significant especially with GaN FET, because maximum gate voltage is as low as 6V. High loop inductance can cause as high gate voltage overshoot that breaks the GaN FET. Inductance between gate driver and GaN FET is mainly depended on length and width of PWB trace and therefore driver and switching device should be placed as close as possible to avoid high overshooting.

Power loop considerations

Current loop in PWB with high frequency and high current is challenging task in the name of EMI and system overall performance. Alternating current in loop produces magnetic field that induces secondary currents in circuit elements close to it and possibly causes adverse effects. Current loop inductance is also determinant in voltage overshoot that can be seen in switching devices. High frequency content that can cause EMI is originated from fast rise times of current pulses. Next here is introduced three different approaches in order to minimize current loop physical size and loop inductance. All these approaches are based on material presented by Efficient Power Conversion [14].

Lateral power loop

In lateral power loop approach fig.25 the main power loop is on single layer, typically on the top layer where also input capacitors C_{in} are mounted. Loop area is determined by component package area. In this approach first inner layer of PWB stack is reserved for shielding layer. Power loop on top layer produces magnetic field that induces current in shielding layer that is opposite to power loop current. Opposite direction flowing currents produces magnetic fields that cancels each other in some measure and makes loop inductance smaller. Distance between top layer and shielding layer should be as small as possible to intensify magnetic field cancellation. Drawback in using shielding layer is losses caused by eddy currents in shield layer.

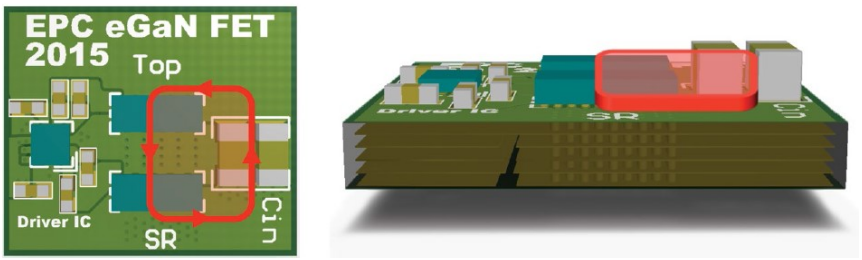

Figure 25 Lateral power loop. Image source: http://epc-co.com/epc/Portals/0/epc/documents/papers/Optimizing%20PCB%20Layout%20with%20eGaN%20FETs.pdf

Vertical power loop

Vertical power loop in fig.26 can be utilized if two sided component assembling is possible. Effective power loop is minimized by guiding current flow through PWB by a set of vias. Input capacitors C_{in} are located on the bottom layer. In this approach there are no shielding layer and instead of that magnetic field self-cancellation is used as current flows in opposing directions in top layer and bottom layer. In order to minimize loop inductance PWB thickness should be as small as possible.

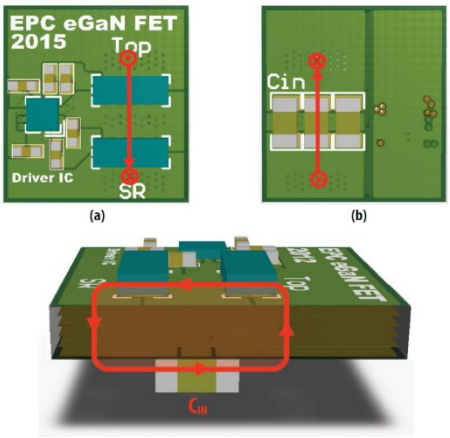

Figure 26 Vertical power loop. Image source: http://epc-co.com/epc/Portals/0/epc/documents/papers/Optimizing%20PCB%20Layout%20with%20eGaN%20FETs.pdf

Optimal power loop

Optimal power loop shown in fig.27 provides the smallest physical loop area. Magnetic field self-cancellation is very effective as distance between incoming and going current is the smallest possible. Capacitors C_{in} are located on the top layer very close to the top side switch drain. PWB thickness do not affect power loop inductance at all.

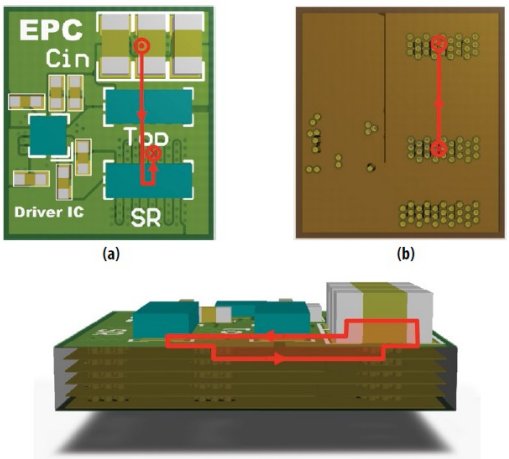

Figure 27 Optimal power loop. Image source: http://epc-co.com/epc/Portals/0/epc/documents/papers/Optimizing%20PCB%20Layout%20with%20eGaN%20FETs.pdf

Fig. 27 shows interleaved switch node and ground polygons which are duplicated on the bottom layer. It achieves reduction in length of high frequency and high current power loop as well as reduction in conductive losses.

Common source inductance

Common source inductance (CSI) is parasitic inductance that is shared with driver circuit gate-source current loop and main power current loop in power converters. CSI is typically a result from switching device internal bonding wire and lead frame stray inductance and PWB layout interconnections inductance. CSI together with gate resistor R_G, gate capacitance C_{GS} and driver internal resistance R_{Sink} can form an LCR resonator fig. 28, which can be seen as a ringing in gate voltage. This ringing can unintentionally turn the device on again at the end of turn-off transition. By increasing gate resistor R_G value ringing can be damped, but same time Miller-turn on possibility is rising. [9]

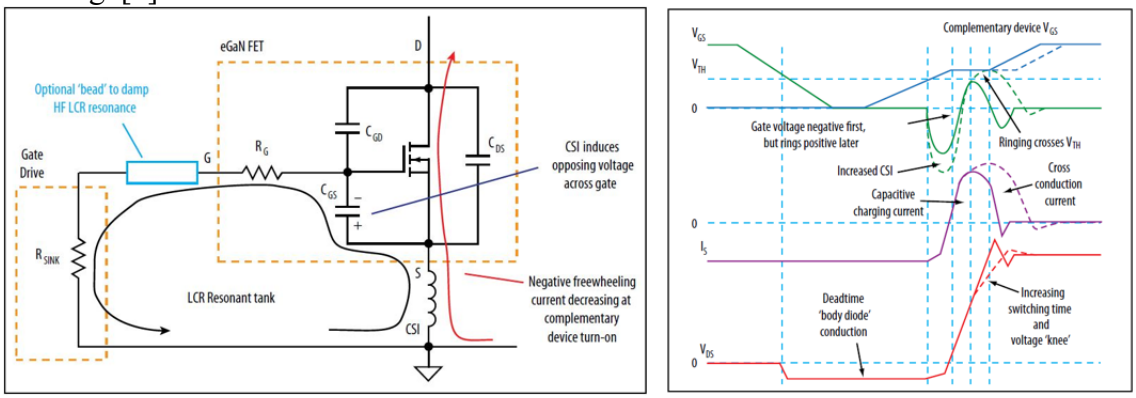

Figure 28 Common source inductance. [9]

CSI induces a voltage that is opposed to the gate drive voltage. CSI increases switching losses as it slows down both turn-on and turn-off transitions of the switch. CSI is more critical to GaN FET than traditional MOSFET because of typically higher di/di and du/dt. As we deal here with GaN FET which LGA package parasitic are very small, common source inductance minimization is therefore layout design issue. [9]
A major factor in GaN FETs excellent performance is package or enclosure that minimizes parasitic elements and allows footprint that helps to make optimal layout design. Interleaving source and drain pads generates small loops with opposing current flow leading into magnetic field self-cancellation and smaller Common Source Inductance. In fig.29 the full advantage of magnetic field self-cancellation is taken. As we see in lower fig.29, magnetic self-cancellation is effective in vertical structures also.

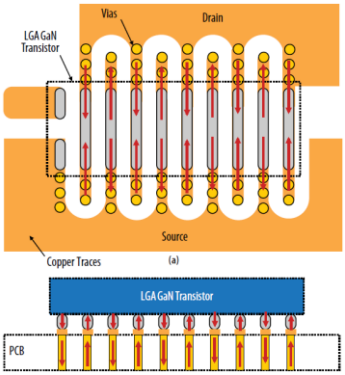

Figure 29 Magnetic field self-cancellation effect. Image source: www.epc-co.com

4.4 EMI

In the following chapter different electromagnetic interference coupling ways are looked over. Fundamental principles how designer can affect electromagnetic interference coupling are discussed and some common methods that are used to suppress noise in circuit are introduced. There are four different ways how electromagnetic interference can couple into electrical system:

1) conductively by galvanic contact
2) inductively by magnetic field
3) capacitively by electric field
4) by radiating electromagnetic waves

Usually in low frequencies the most important noise coupling occurs via galvanic connection. Inductive coupling can be reduced by slowing down current transitions di/dt and keeping current loop areas small. Capacitive coupling can be reduced by slowing down voltage transitions du/dt and making capacitances between interference circuits smaller, by shrinking circuit physical size or increasing the distance between interfering sub circuits. In general radiating interference is managed mainly by keeping circuit elements much smaller than noise frequency wavelength λ or alternatively noise operation frequency is decreased if possible. When circuit elements dimension $d < \frac{\lambda}{20}$ there should not be radiated interference on that frequency [15]. At 6.78 MHz critical dimension is

$$d = \frac{\lambda}{20} = \frac{c}{f_{sw} * 20} = \frac{2{,}998 * 10^8 \frac{m}{s}}{6{,}78 * 10^6 Hz * 20} = 2{,}21m\ .$$

Clearly the harmonic content reach much higher frequencies and therefore also smaller circuit dimension are coming interesting as potential EMI source. The largest dimension in the WPT system dealed here can be found from source coil which size is 21 cm x 14 cm. By using the above expression an approximation for frequencies that such current loop will radiate can be found as follows

$$f_{rad} \geq \frac{c}{d * 20} = \frac{2{,}998 * 10^8 \frac{m}{s}}{0{,}21m * 20} = 71MHz$$

Electromagnetic interference or noise in electronic circuit can be classified into differential mode or common mode noise according to the conducting way. Differential mode noise couples into the circuit same way as usage signal, current is flowing in opposite directions in signal wire and ground. Fig. 30 visualizes differential mode noise in circuit and show fundamental method i.e. LC-filter to suppress it.

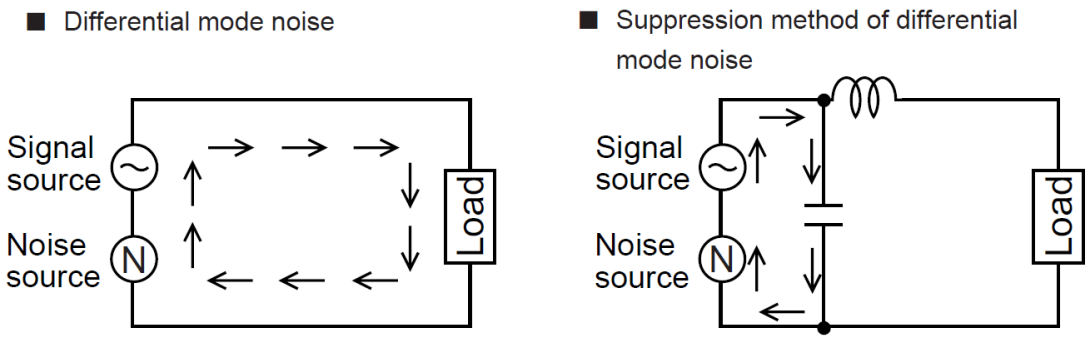

Figure 30 Differential mode noise and suppression method. Image source: http://www.murata.com/~/media/webrenewal/products/emc/emifil/knowhow/26to30.ashx

Common mode noise couples into the circuit at least one other coupling way than the usage signal do fig. 31, typically in capacitive or inductive way. If coupling bath can't be severed totally, common mode noise coupling can be reduced by increasing the coupling bath impedance. Common mode noise occur typically as voltage between two different ground points in the system. Voltage difference can be consequence of current flowing in ground plane or there might be inductively coupled noise in loop formed by signal wires and ground. Fig. 31 right, shows typical suppression method for common mode noise, a common mode filter.

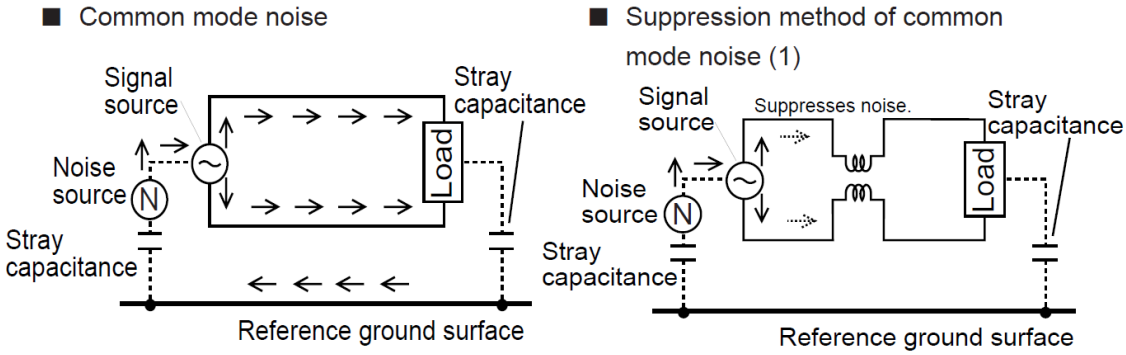

Figure 31 Common mode noise and suppression method. Image source: http://www.murata.com/~/media/webrenewal/products/emc/emifil/knowhow/26to30.ashx

Common mode filter seen in fig. 32 is typically made from two equally wounded coils around toroidal ferrite core. When coils are symmetrically wounded and coupling between them is very tight, filter means high impedance for common mode noise and very small impedance for differential mode noise.

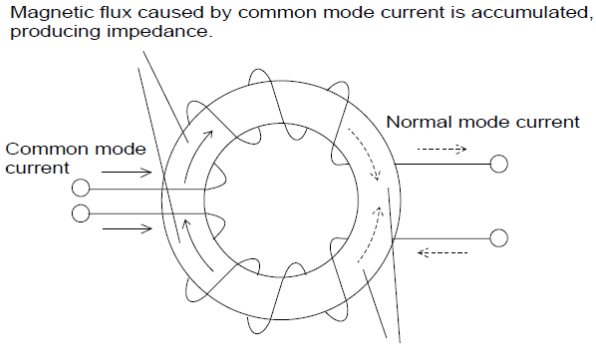

Figure 32 Common mode choke. Image source: http://www.murata.com/~/media/webrenewal/products/emc/emifil/knowhow/26to30.ashx

$$Z_{CM} = k(L + M)$$
$$Z_{DM} = k(L - M)$$

In above expressions L is coil inductance, M is mutual inductance between coils and coupling factor k. In common mode filter coupling factor k is very close to one leading to fact $L = M$ and further meaning high impedance for common mode current and low impedance for differential mode current.

It is important to identify noise type, differential or common mode, when suppression method is selected. Noise suppression method that works well with differential mode noise is not working at all with common mode noise and vice versa. Wrong type of suppression method can make EMI even worse. When trying to get rid of differential mode noise, there is a risk that differential mode noise is transformed into common mode noise which can be even more difficult problem to solve. [15]

Definitely best way to concern EMC issues is to try avoid as much as possible beforehand by good circuit and layout design. In the beginning of the design process the means available to handle EMI issues are more diverse. The further the design process has progressed, the less are means available that works against EMI and that expensive they usually are. The well-known principles to mitigate EMI are:

- keep pulse rise times as low as possible
- reduce frequency if possible
- decrease current that flows in current loop
- reduce the loop area.

Next are shown how spectral content of a trapezoidal voltage wave (fig. 33) can be calculated by using Fourier series. Derivation of following expression are bypassed as those are founded in several signal processing dealing sources in literature, like [15].

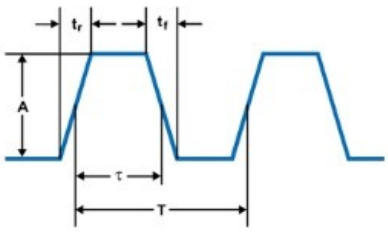

Figure 33 Trapezoidal waveform. Image source: http://www.ecnmag.com/article/2009/10/designing-emc-compliant-automotive-switching-buck-regulator

Fourier series, where $n = 1,2,3 \ldots$:

$$C_n = A\frac{\tau}{T}\left(\frac{\sin(\pi n f_0 \tau)}{\pi n f_0 \tau}\right)\left(\frac{\sin(\pi n f_0 t_r)}{\pi n f_0 t_r}\right)e^{-j\pi n f_0(\tau+\tau_r)}$$
$$f_0 = \frac{1}{T}$$

Envelope curve of Fourier series:

$$V_k = 2A\frac{\tau}{T}\left|\frac{\sin(\pi f \tau)}{\pi f \tau}\right|\left|\frac{\sin(\pi f t_r)}{\pi f t_r}\right|$$

In fig. 34 is plotted the envelope curve of Fourier series calculated for trapezoidal wave with fundamental frequency 6.78MHz and 50% duty cycle. The blue curve is very much

like pure square wave with 1ns rise time, even harmonics are absent. The red curve represents trapezoidal wave with 15ns rise time. In red curve there can be seen pretty high 2nd harmonic and 4th is as high as the 5th harmonic.

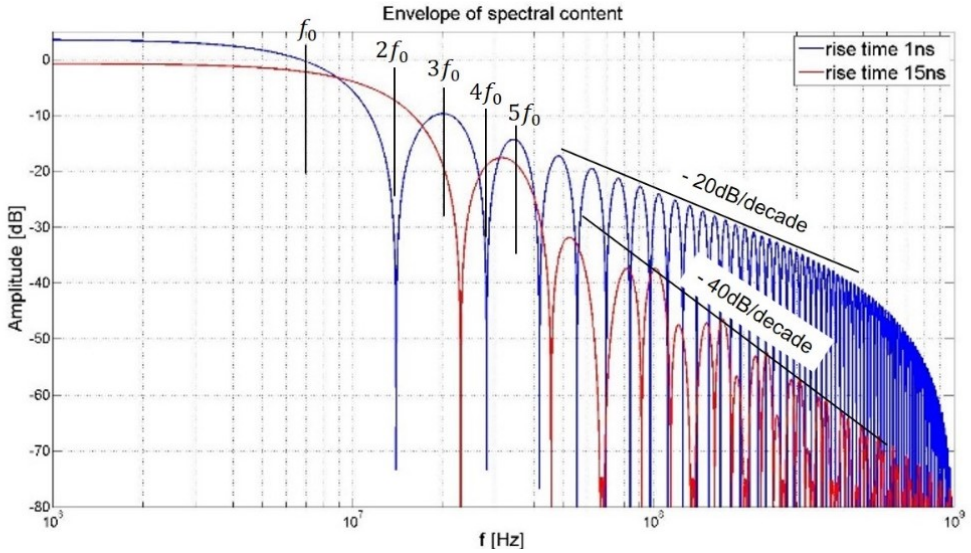

Figure 34 Envelope curve of trapezoidal waveform Fourier series.

Longer rise time means that high frequency components are dying faster, but significant even order harmonics will be seen at lower frequencies. Fig.35 below clarify the meaning of increased rise time. After first corner frequency $f_1 = \frac{1}{\pi\tau}$ harmonics are dying at speed of $-20dB/dec$. The second corner frequency $f_2 = \frac{1}{\pi t_r}$ is determined by rise time t_r, after f_2 harmonics are dying $-40dB/dec$. Increasing the rise time shift the second corner frequency f_2 to the lower frequencies, leading to that high order harmonics are dying faster.

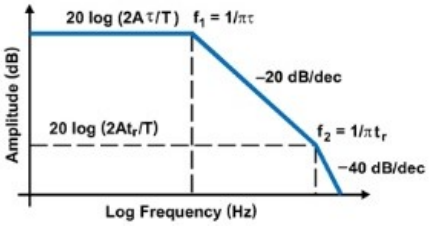

Figure 35 Rise time effect on harmonic frequency attenuation. Image source: http://www.ecnmag.com/article/2009/10/designing-emc-compliant-automotive-switching-buck-regulator.

As a rule of thumb, harmonic frequency components coming from edges of square pulse that have remarkable energy can be approximated 0,4 divided by rise time [15]:

$$\frac{0{,}4}{15ns} = 27\ MHz \qquad \frac{0{,}4}{1ns} = 400\ MHz$$

Simple calculations prove the fact that slowing down square wave rising and falling edges have great impact in reducing harmonic components. Increasing rise time from 1ns to 15ns reduces troublesome harmonic frequency bandwidth more than one decade. In fig. 36 is one example of EMI filter which combines common mode choke and LC-filter into SMD type package. In left side is shown circuit schematic of filter and right side shows over 60 dB attenuation at 4 MHz - 150 MHz frequency band.

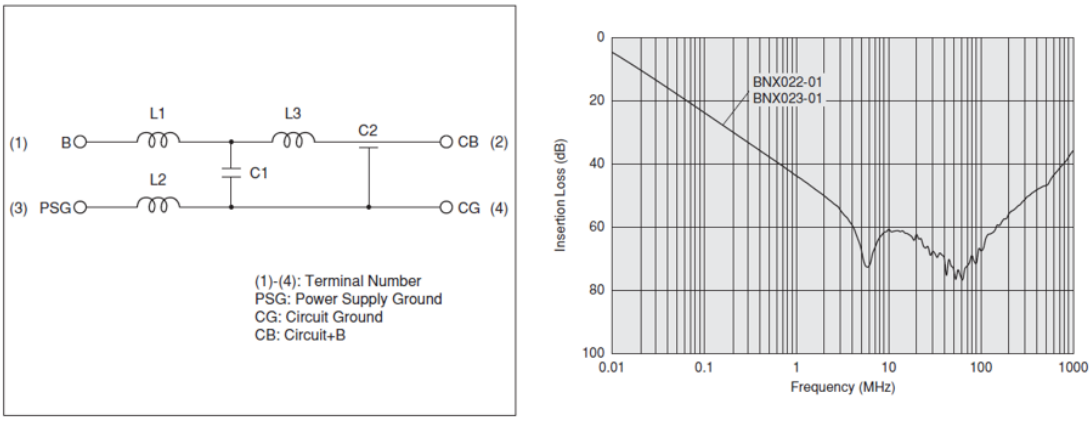

Figure 36 EMI filter candidate. Image source: http://www.murata.com/~/media/webrenewal/support/library/catalog/products/emc/emifil/c31e.ashxf

5 Power amplifier design and implementation

As we are dealing here with power transfer, high operating efficiency is the most important selection criterion for amplifier topology. Therefore all amplifier topologies discussed here are switching-based and such that soft-switching techniques can be utilized. Other issues where attention is paid when selecting suitable amplifier topology are EMI performance and susceptible to the load variation. In following Class D, E and F amplifier topologies are introduced. Selection criteria for topologies Class D ZVS and Class E to be later designed and implemented are discussed.

Reflected impedance in fig.37 is simplified model of entire coil network between source side power amplifier and device side DC load resistance [16]. Reflected impedance $Z_{load} = R_{load} + jX_{load}$ is complex impedance with real- and imaginary-parts. This simplification is used later in amplifier schematics in this chapter. If later in this work R_{DCload} is mentioned, then it is discussed about DC load resistance in receiver side.

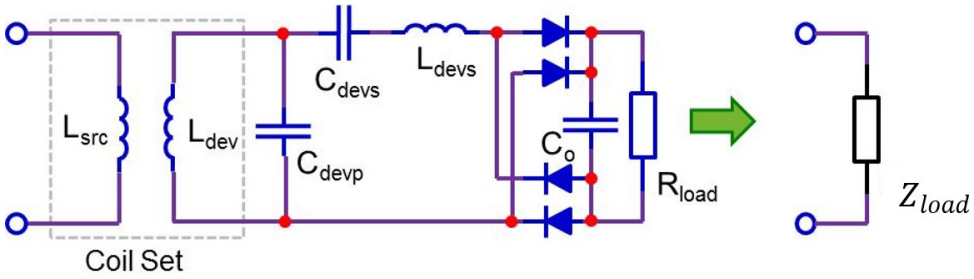

Figure 37 Reflected impedance. [16]

5.1 Amplifier topology selection

Class D

Fig. 38 below shows fundamental voltage mode Class D power amplifier in WPT system and its ideal switch node waveforms. Half-bridge configured switches Q_1 and Q_2 forms square pulse train which is smoothened close to sinusoidal in output filter formed by L_m and C_m.

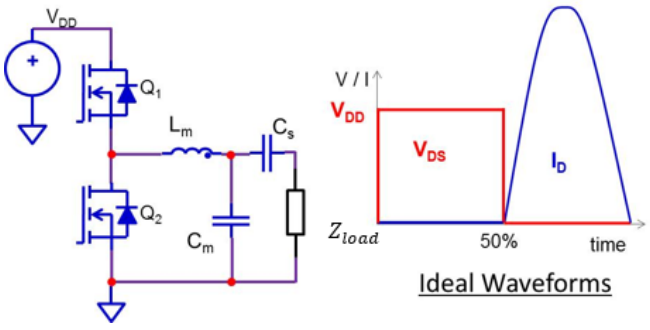

Figure 38 Basic structure of Class D power amplifier in WPT. [16]

In Class D amplifier switching device output capacitance C_{oss} is predominant loss source. After every switching cycle charge from output capacitance C_{oss} need to be discharged through FET's conducting channel where R_{DSon} turns the flowing current into power loss. In order to reduce Class D amplifier switching device output

capacitance C_{oss} loss, ZVS modification is introduced in fig.39. ZVS tank circuit is used to self-commutate voltage transition in switching device, negative current I_{LZVS} is used to discharge charge in C_{oss} before switch is turned on. Advantage of parallel type ZVS tank circuit is that ZVS operation is immune to R_{load} variations, load current is not affecting the current flowing in ZVS tank circuit. [16]

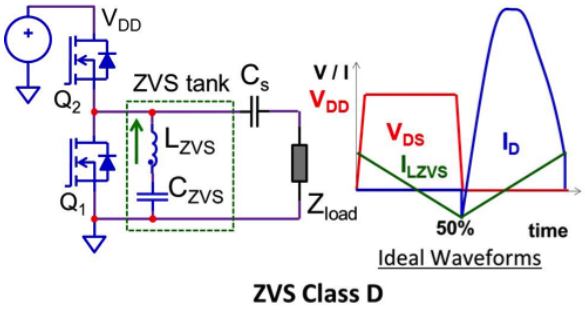

Figure 39 Class D ZVS power amplifier for WPT. [16]

Class D amplifier needs two switching devices and fundamentally switching losses are twice as high as in amplifier which need only one switch. In addition more complex driver circuit is needed and losses in driver may be also higher. Ideally switching device voltage rating is same as supply voltage V_{DD} which can be seen as advantage of Class D.

Class E

For the first time this amplifier class was introduced by Sokal & Sokal [17] in 1975. High interest to improve radio transmitter power stage efficiency led to the development of new type of amplifier. Like in Class D amplifier, to achieve high efficiency the Class E amplifier attempts to minimize the power dissipated in active switching device. In Class E switching device parasitic capacitance C_{oss} is taken part of load network seen in fig. 40. Before device is turned on, output capacitance C_{oss} and parallel shunt capacitance C_1 are fully discharged. Energy stored to C_{oss} and C_1 is moved to load network's inductance L_2, making it possible to switch the device on in no-voltage condition.

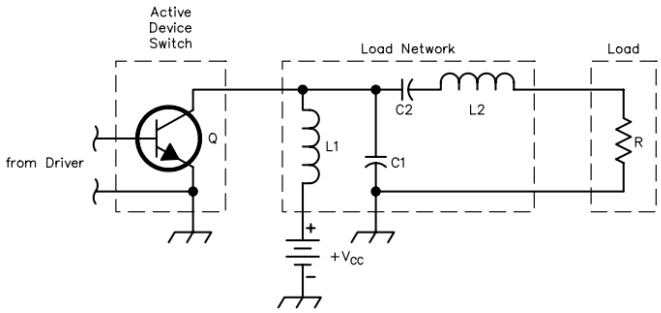

Figure 40 Class E amplifier schematic that was introduced by Sokal & Sokal in 1975. [17]

In load network capacitor C_2 is used to tune out the reactive component of reflected load and concurrently offering a DC block. Inductor L_1 is dimensioned to offer constant current into circuit and its design is based on the allowable ripple characteristics. In several references inductor L_1 is called RF Choke as its function is to decouple DC supply from high frequency voltage in switching device. Inductors L_1 and L_2 are in main current path, thus increasing losses. Advantage of Class E amplifier is that only

one active switching device is needed, simple a ground referenced gate driver can be used. Drawback of Class E is that voltage rating for switching device is high. Theoretical value for drain voltage $V_{DS} = 3{,}56 * V_{DD}$. Fig. 41 shows ideal wave forms in Class E amplifier.

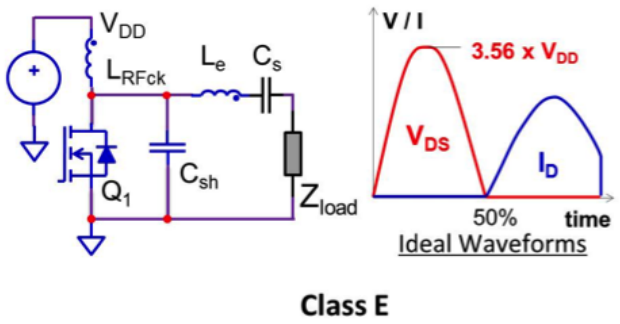

Figure 41 Class E power amplifier in WPT. [16]

Class E amplifier load network tuning is sensitive to the load resistance variations. The load resistance variations affects the current that is drawn out of amplifier and alters the voltage transitions in switching device such that ZVS operation is spoiled, thus tuning the Class E amplifier for wide impedance range is challenging.

Class F

Class F amplifier in fig.42 consists several harmonic frequency resonators that are used to shape switching device drain-voltage and drain-current waveforms. Adding harmonic content into waveforms effectively flattens drain voltage and allows current flow mainly in absence on voltage i.e. ZVS operation. Theoretically as high efficiency as Class E is possible but output network tuning is more challenging task. [18]

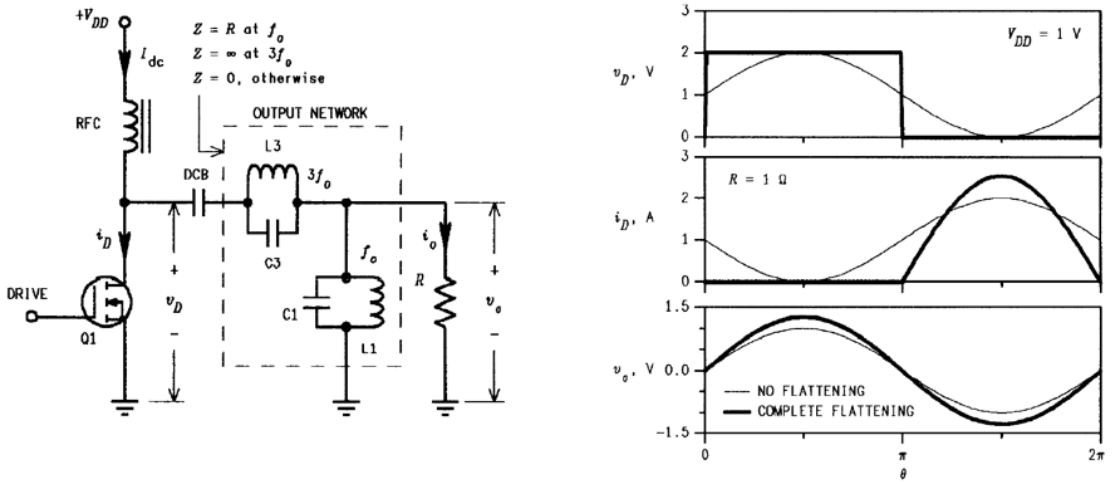

Figure 42 Class F power amplifier schematic and ideal wave forms. [18]

Selected amplifier topologies

The Class D ZVS was other amplifier topology that was selected for design and implementation during this work. In addition to the high efficiency expectation, main selection criterion for Class D ZVS was its ability to operate under varying loading conditions. Even though Class E amplifier is vulnerable to load variation it was selected to be second amplifier to implement. Its simple structure with only one switching device is attractive, simple driver circuit is enough and no need to adjust dead-time like in Class D. Load network in Class E appeared to be easier tune than with Class F and more references that mention Class E in WPT system were available [16][19].

5.2 Class D ZVS

Block diagram in fig.43 shows main components of Class D ZVS power amplifier. The full circuit schematic, PWB layout and BOM of the design are shown respectively in Appendix A, B and C.

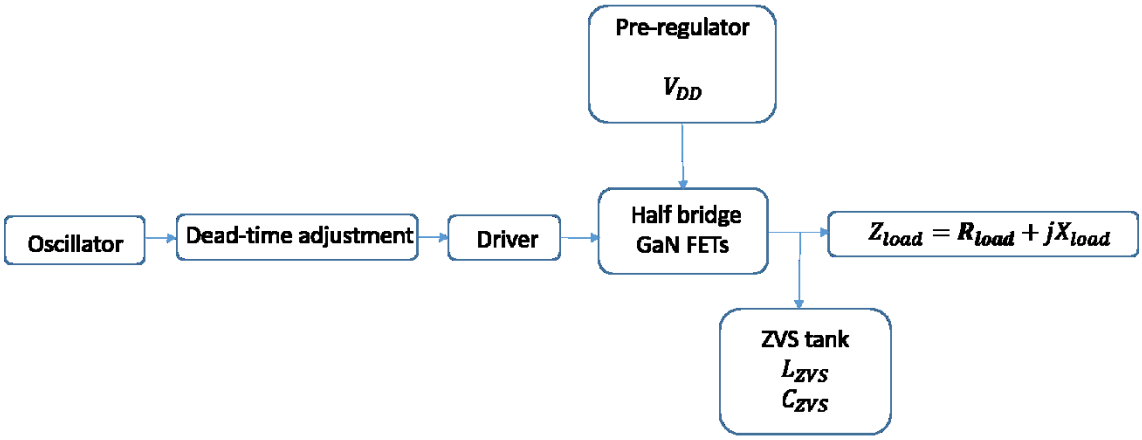

Figure 43 Class D ZVS block diagram.

Design specifications and critical component selection

The starting point of the design was A4WP compliant transmitter and receiver coil set which was available for this work. The coil set included Class 3 source coil with nominal output power $P_{TX,in} = 16W$ and Category 3 receiver coil with nominal output power $P_{RX,out} = 6{,}5W$. The source coil's maximum RMS current was given to be 800mA. However, from the beginning it was clear that while the performance of the amplifier later will be tested those nominal values are going to be just some reference values that are exceeded above and below. At this point of the design there will be no feedback loop between the output and input of the circuit, the design will be open-loop system. The output power will be controlled by the voltage supplied to the amplifier.

To calculate needed operation voltage V_{DD} design equation for Class D ZVS given in [16] was used. The calculation for needed operation voltage is based on reflected load resistance value R_{load} and the required output power P_{load}. Here 75% power transfer efficiency is assumed. The target output power P_{load}

$$P_{load} = 16W * 0{,}75 = 12W.$$

$$V_{DD} = \sqrt{\frac{\pi^2 * R_{load} * P_{load}}{2}} = \sqrt{\frac{\pi^2 * 10\Omega * 12W}{2}} = 24{,}33V$$

Because the reflected impedance Z_{load} and its real part R_{load} is difficult to measure, here in calculations is used approximation value $R_{load} = 10\Omega$. Calculations afterwards from measurements showed that value for R_{load} is in range 6 - 12Ω on depending on R_{DCload} variation.

Switching device selection

In theory voltage rating for switching device with Class D ZVS is the same as supply voltage V_{DD}. Yet, some safety margin is reasonable to add if some unexpected supply voltage peaking occurs or there might appear overshoot and ringing in V_{DS} voltage wave form during testing procedures. Here switching device with $V_{DS} = 40V$ voltage rate was selected.

In general low gate charge is preferred when high switching speeds are intended to use. Switching device gate charge and driver circuit current sourcing capability determines how fast switch can be eventually turned on. There is always trade of between R_{DSon} value and paracitic capacitances of the switching device. Making physical structure smaller parasitic capacitances can be reduced but same time resistance in conducting channel is increasing. Because in this amplifier design it is was intended to use zero voltage switching, gate charge do not need to be extremely small. In table 2 is shown selection of suitable GaN FETs for this amplifier design.

Table 2 Selecting table for GaN FET. Source: www.epc-co.com

Part Number	Configuration	V_{DS}	Max $R_{DS(ON)}$ (mΩ) @5V_{GS}	Q_G typ (nC)	Q_{GS} typ (nC)	Q_{GD} typ (nC)	Q_{OSS} typ (nC)	Q_{RR} (nC)	I_D(A)	LGA Package (mm)
EPC2023	Single	30	1.3	20	5.8	1.9	28	0	60	6.1 x 2.3
EPC2024	Single	40	1.5	19	6.4	2	32	0	60	6.1 x 2.3
EPC2030	Single	40	2.4	18	5.2	3.4	41	0	31	4.6 x 2.6
EPC2015	Single	40	4	10.5	3.0	2.2	18.5	0	33	4.1 x 1.6
EPC2015C	Single	40	4	8.7	3.0	1.4	19	0	36	4.1 x 1.6
EPC2014C	Single	40	16	2.0	0.70	0.30	4	0	10	1.7 x 1.1
EPC8004	Single	40	110	0.370	0.120	0.047	0.63	0	2.7	2.1 x 0.85

At ZVS operation the output capacitance of switching device C_{OSS} is absorbed into matching circuit or ZVS tank circuit as it is a case with Class D ZVS amplifier. Here expression below is given as handy tool to compare different switching device suitability for ZVS amplifier. In FOM_{ZVS} expression $R_{DS,on}$ unit is expected to be $m\Omega$ $Q_{G,GD}$ unit nC. [9]

$$FOM_{ZVS} = R_{DS,on} * (\mathrm{Q_G} - \mathrm{Q_{GD}})$$

EPC2015: $FOM_{ZVS} = 4 * (10{,}5 - 2{,}2) = 33$

EPC2014C: $FOM_{ZVS} = 16 * (2 - 0{,}7) = 21$

As above calculation show that EPC2014C would be optimal choice, still EPC2015 was selected because it has attractive low R_{DSon} value and its physical dimension are more suitable for handmade assembling. To make comparison with MOSFET, FOM_{ZVS} was calculated for Infineon OptiMOS™ with comparable electrical characteristic table 3. Infineon OptiMOS™ is known state-of-art switching power MOSFET product.

Table 3 Comparable MOSFET devices.

Part	V_{DS} [V]	$R_{DS,on}$ $[m\Omega]$	Q_G $[nC]$	Q_{GD} $[nC]$	Q_{RR} $[nC]$	I_D [A]	Package [mm]
BSC026N04LS	40	2,6	32	5,2	57	100	5,0x6,0
BSZ097N04LS	40	8,1	18,0	1,9	15	40	5,0x6,0

BSC026N04LS: $FOM_{ZVS} = 2{,}6 * (32 - 5{,}2) = 70$

BSZ097N04LS: $FOM_{ZVS} = 8{,}1 * (18{,}0 - 1{,}9) = 130$

Even though above shown comparison is very simple, some conclusions can be drawn about GaN FET superior switching characteristics against MOSFET.

Driver circuit

Texas Instrument gate driver LM 5113 [12] is specified to drive both high-side and low-side switches in half bridge connected GaN FETs and it is equipped with internal voltage clamping to ensure that $V_{GS,max}$ is not exceeded in any conditions. In addition LM5113 is equipped with splitted output where pull-up and pull-down connections are separated to make it possible to adjust both current paths individually. To achieve optimal gate driving and to prevent unwanted events like voltage ringing and Miller turn on, pull-up and pull-down resistors can be adjusted separately. Driver circuit driving capability and suitability for particular switching device can be approximated if driver peak source current and switching device gate charge are known and making use of the simple equation $Q = time\ x\ current$.

EPC2015 GaN FET gate charge: $Q_G = 11{,}6nC$
LM 5113 peak source current: $I_{driver} = 1{,}2A$

From gate charge Q_G and driver peak source current the minimum time $t_{on,min}$ that is needed to switch device on can be calculated.

$$t_{on,min} = \frac{Q_G}{I_{driver}} = \frac{11{,}6nC}{1{,}2A} = 9{,}67ns$$

Later testing proved that even faster switching time is possible with this driver, but as ZVS operating amplifier was intended to design extremely fast voltage rise times were even not needed. In hard switching topologies short switching times are definitely preferred when switching losses are remarkable and therefore driver current sourcing capacity is therefore more important. Few external components that are needed along with LM5113 were dimensioned, bypass capacitor C_{VDD} between pin V_{DD} and ground and bootstrap capacitor C_{BST} that is needed to provide high-side switch gate charge. For brevity calculations are not shown here.

Gate drive loop inductance

Gate drive loop inductance is significant especially with GaN FET, because maximum allowed gate voltage is as low as 6V. High loop inductance can cause as high gate voltage overshoot that breaks the GaN FET. Inductance between gate driver and GaN FET is mainly depended on length and width of PWB trace and therefore driver and switching device should be placed as close as possible to avoid high overshooting. Following equation (36) gives maximum value for gate drive loop inductance L_G [20].

$$\frac{1}{4} * \left(R_G + R_{gate} + R_{pull-up}\right)^2 * C_{GS} \geq L_G \tag{20}$$

In equation (20) R_G is GaN FET's internal gate resistance, discrete gate resistance R_{gate} and internal driver pull-up resistance $R_{pull-up}$, C_{GS} is GaN FET gate-to-source capacitance. Needed value for R_{gate} can be calculated with () below.

$$R_{gate} \geq \sqrt{\frac{4L_G}{C_{GS}}} - R_G - R_{pull-up}$$

To calculate R_{gate} inductance between driver and switching device need to be approximated. Inductance of PWB trace is proportional to the length of the trace and inversely proportional to the width of the trace. Equation to calculate trace inductance [21]:

$$L \cong 2 \ln \frac{5{,}98 * h}{0{,}8 * w + t} \quad \left[\frac{nH}{cm}\right]. \tag{21}$$

From designed Class D ZVS layout:
Trace length between driver and gate: $l = 10mm = 1cm$
Trace width: $w = 0{,}7mm = 0{,}07cm$
Distance between trace and ground plane: $h = 0{,}5mm = 0{,}05cm$
Copper thickness: $t = 35\mu m = 0{,}0035cm$

From EPC2015 datasheet [22] and driver circuit datasheet [12]:

$$C_{GS} = 515pF$$
$$R_G = 0{,}6\Omega$$
$$R_{pull-up} = 2{,}1\Omega.$$

Loop inductance between driver and gate calculated with equation (21):

$$L_G = 2 \ln \frac{5{,}98 * h}{0{,}8 * w + t} l = 2 \ln \frac{5{,}98 * 0{,}05}{0{,}8 * 0{,}07 + 0{,}0035}\ 1cm = 3{,}23\ nH$$

Calculated gate resistance (0603 resistor on board) while loop inductance $L = 3{,}23nH$:

$$R_{gate} \geq \sqrt{\frac{4L_G}{C_{GS}}} - R_G - R_{pull-up} = \sqrt{\frac{4 * 3{,}23nH}{515pF}} - 0{,}6\Omega - 2{,}10\Omega = 2{,}31\Omega$$

In design R_{gate} ended up to be 2.2Ω for both high and low-side GaN FET. The chosen driver package WSON-10 pin configuration is such that it is not possible to shorten significantly the trace length between driver and gate in layout. Smaller outlined DSBGA package that is available would be more optimal when extremely short distance is needed between driver and switching device gate. Another option to reduce loop inductance is to widen the trace. Effective way to reduce loop inductance and keep gate resistance low is to design loop trace short and wide. Low gate resistance is desirable when fast switching speed is needed.

ZVS tank circuit

Inductor L_{ZVS} in ZVS tank circuit was calculated by design equations given in [16].

$$V_{DD} = \sqrt{\frac{\pi^2 * R_{load} * P_{load}}{2}}$$

$$C_{OSSQ} = \frac{1}{V_{DD}} * \int_0^{V_{DD}} C_{OSS}(V_{DS})\, dv_{DS}$$

$$L_{ZVS} = \frac{\Delta t_{vt}}{8 * f_{sw} * \left(2 * C_{OSSQ} + C_{well}\right)}$$

To calculate C_{OSSQ} design equation was given in [16]. In fig.44 C_{OSSQ} value was determined as shaded area from graph taken from datasheet [22].

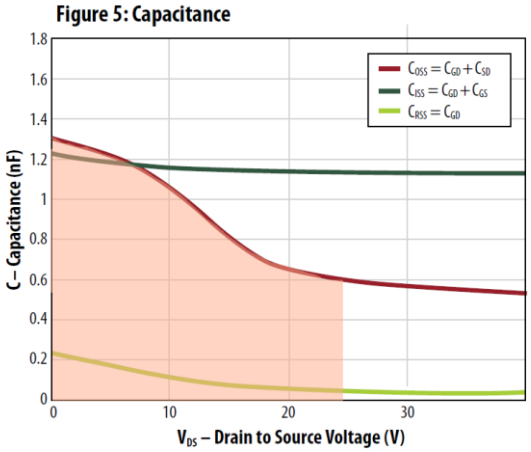

Figure 44 Parasitic capacitances in function of drain-to-source voltage. [22]

$$C_{OSSQ} = \frac{1}{V_{DD}} * \int_0^{V_{DD}} C_{OSS}(V_{DS})\, dv_{DS}$$

$$C_{OSSQ} = \frac{1{,}2nF * 10V + 0{,}8nF * 10V + 0{,}6nF * 4{,}33V}{24{,}33V} = 929pF$$

In equation (22) $\Delta t_{vt} = 15ns$ is switch node voltage transition time, $C_{well} = 40pF$ is gate driver well capacitance given in [23], $f_{sw} = 6.78MHz$ is switching frequency and C_{OSSQ} is equivalent output capacitance of switching device.

$$L_{ZVS} = \frac{\Delta t_{vt}}{8 * f_{sw} * (2 * C_{OSSQ} + C_{well})} = \frac{15ns}{8 * 6{,}78 * 10^6 \frac{1}{s} * (2 * 929pF + 40pF)} = 149nH \qquad (22)$$

The capacitor C_{ZVS} value is not especially critical because ZVS tank circuit is not operating in resonance. The capacitor C_{ZVS} has mainly affect on voltage ripple and therefore it can be chosen relatively loosely. In experiments $C_{ZVS} = 1uF$ seemed to work well.

Oscillator

To get needed 6.78MHz switching frequency Linear Technology LTC6908-1 silicon oscillator was chosen. Frequency is programmed by a single external resistor or alternatively frequency is set by current or voltage source. This oscillator type was selected because it has two 180° phase shifted 50% duty cycle square wave outputs, which means an easy connection to the driver circuit without external logic gates.

Pre-regulator

In order to increase security and to prevent accidental destruction of components during the development process, the amplifier board was outfitted with pre-regulator. The purpose of protection is to limit the current and voltage supplied to the power amplifier i.e. half bridge connected GaN FETs. The pre-regulator is based on Linear Technology LT3741 buck controller. The controller is designed in order to control accurately output current and voltage. One criterion for the choice of this model was its ability to de-rate the maximum allowable current based on the temperature raise in the circuit board.

Dead-time adjustment

The dead-time is defined here as a measured time interval from the point when the turn-off device (e.g. high-side FET) gate voltage is reduced to gate threshold voltage V_{TH} to the point when turn-on device (e.g. low-side FET) gate voltage is reaches the gate threshold voltage V_{TH}. It is important to measure dead-time in real gate voltages in the presence of operating switching devices. The dead-time is affected by fluctuation seen in switching device electrical characteristics i.e. loading variations and that is reason why measuring dead-time from gate signal source is inaccurate and meaningless. Variations in gate threshold voltage, device operating voltage, gate resistance and capacitance are affecting dead-time accuracy. In addition to switching device effects on dead-time control accuracy, driver circuit pulse width and phase shift can vary a bit in the function of temperature. [13]
As already has been discussed the absence of body diode in GaN FET and rather high voltage drop over GaN FET during reverse conducting (‘body diode’ operation) can lead into significant losses. Best way to reduce reverse conducting losses is to keep tight dead-time control. Shorter dead-times between switching means shorter reverse conducting intervals and less losses. Features of GaN FET allows very tight dead-time control and definitely it is the thing that should be utilized when trying to achieve high

efficiency levels. However a narrow dead-time adjustment can be problematic because of variation in component values and unexpected shoot-through can occur. It might be necessary to add certain safety margins into dead-time to make mass production possible.

Fig. 45 shows a simple circuit structure that can be used for dead-time control of half bridge based converter topologies. Firstly oscillator's square wave pulse is split into the high-side and low-side phases. 180° phase shift between high-side and low-side is implemented with logic inverter and to keep propagation delay equal in both branches high-side control pulse is lead through buffer. RC-circuit time constant is adjusted to achieve wanted delay in the rising edge of control square wave. Depending on driver circuit input voltage threshold level and rise time of control pulse after RC-circuit dead-time is adjusted. The diode in parallel with resistor is there to make RC-circuit affecting only turn-on edge of the control pulse.

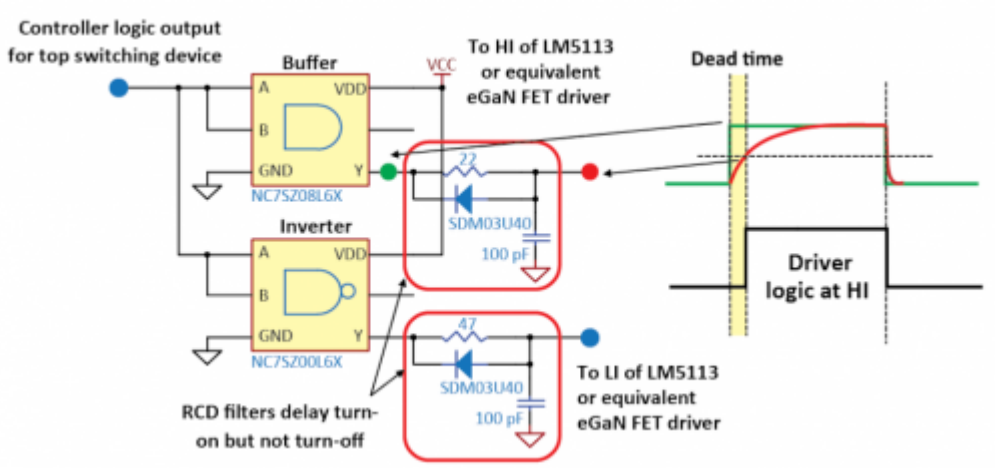

Figure 45 Dead-time control. Image source: http://www.eeweb.com/blog/alex_lidow/how-to-gan-egan-fets-in-high-frequency-buck-converter

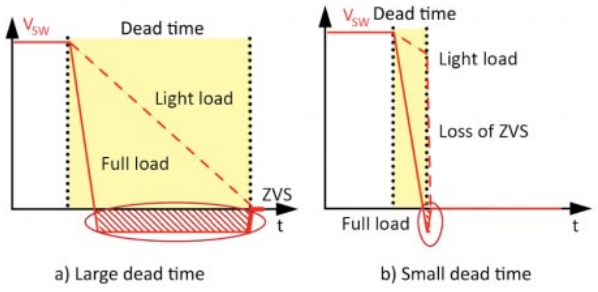

Figure 46 meaning of load current in dead-time adjustment. Image source: http://www.eeweb.com/blog/alex_lidow/how-to-gan-egan-fets-in-high-frequency-buck-converters

In the falling edge switch node voltage transition time is depended on load current. Higher load current can self-commutate switch node voltage to ground faster than lower load current can. In fig. 46 is shown effect of dead-time in light and full load conditions. When fixed dead-time is adjusted under light load conditions ensures that good efficiency in lower power levels but full power operation efficiency is decreased due to increased 'body diode' conducting losses. In other hand, if dead-time adjustment is done under full load, 'body diode' conducting losses are minimized but same time switching losses are increased as ZVS operation is spoiled. Amount of the load current

affects the rising edge only a little or not at all and therefore minimizing dead-time there also minimizes 'body diode' conducting losses. [13]

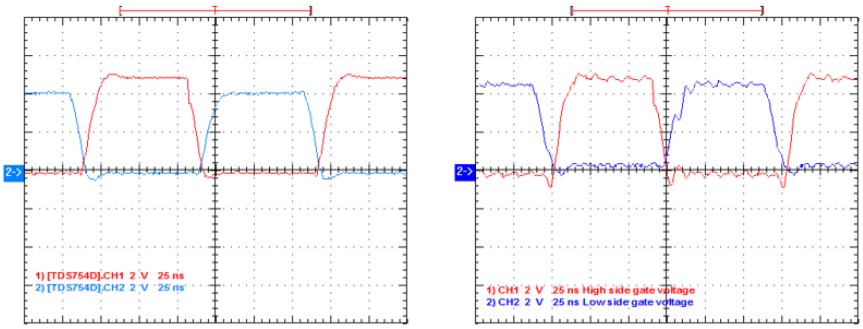

Figure 47 Left: Gate signals when power is off. Right: Gate signals when power on.

Fig. 47 demonstrates the gate signal distortion when power is turned on. Fig.48 shows optimal dead-time adjustment and tuned ZVS operation.

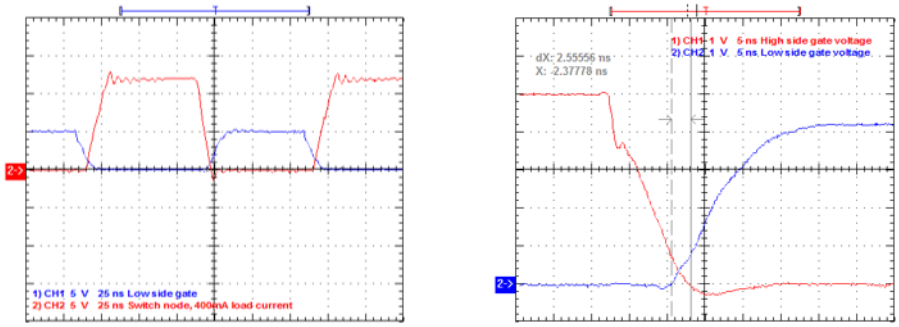

Figure 48 Left: Switch node voltage and gate signal in optimal dead-time adjustment. Right: Example of tight dead-time adjustment.

5.3 Measurements for Class D ZVS

In first part, optimal Class D ZVS tuning is introduced and effect of load variation in switch node wave form is demonstrated. Second part is reserved for performance tests, as a whole three different performance tests were accomplished. At this point the measurement set up is also performed. Third part shows Class D ZVS amplifier thermal performance in three different power level while the last part is reserved for conducted EMI measurements. Fig.49 shows assembled Class D ZVS amplifier board. SMA connector were used to connect source coil to the board.

Figure 49 Assembled Class D ZVS PWB.

ZVS tuning

The ZVS tuning of the amplifier was detected from switch node voltage. Adjustment in practice were performed by adjustable capacitor seen in fig.50. After tuning adjustable capacitor value was measured and replaced with equal discrete capacitor.

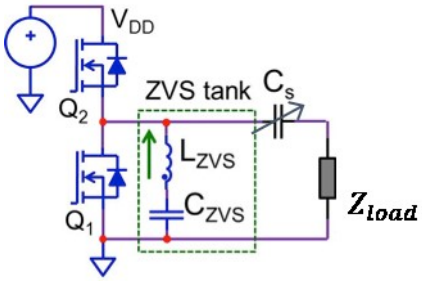

Figure 50 Class D ZVS tuning with adjustable capacitor. [16]

When measuring voltage waveforms which have several MHz frequency and whose harmonic content can reach even several hundred MHz, good practice is to reduce loop that can gather noise in oscilloscope probe. Fig. 51 shows how grounding wire is removed from the probe and grounding is done shortest possible way to PWB. Bandwidth of oscilloscope is recommended to be at least 500MHz, which allows to measure voltage pulses with 1ns rise time accurately.

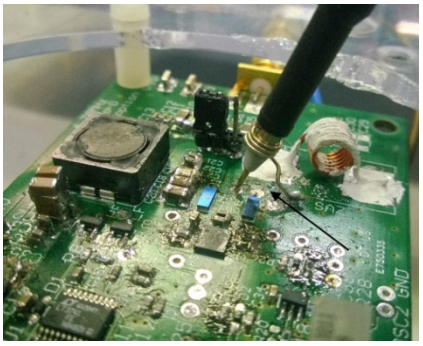

Figure 51 Reduced grounding loop in oscilloscope probe.

Fig.52 shows optimal ZVS tuning in left while right side show warped ZVS action.

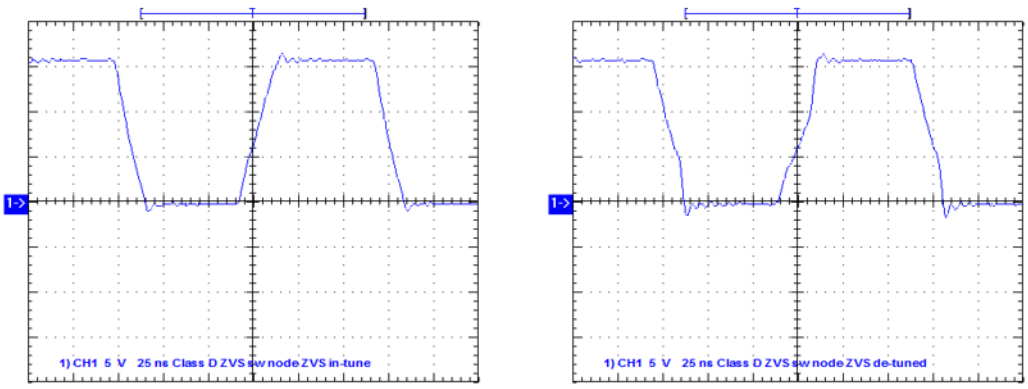

Figure 52 Left: Optimal Class D ZVS adjustment. Right: Out of tune Class D ZVS operation.

Fig. 53 shows DC load resistance variation effect on switch node waveform. ZVS adjustment stays tuned nevertheless loading is varied.

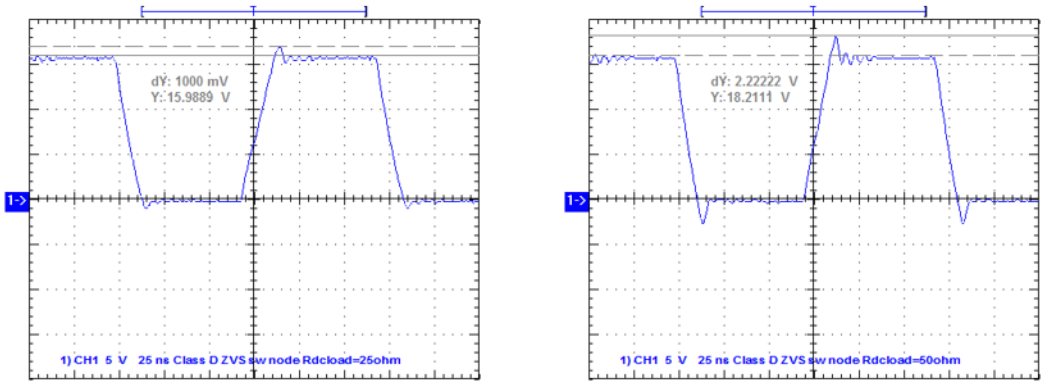

Figure 53 Load resistance variation in switch node wave form.

Fig. 54 shows coil distance effect on switch node waveform. Effect of coil distance variation in switch node waveform is similar to load resistance variation, ZVS tuning is not disturbed.

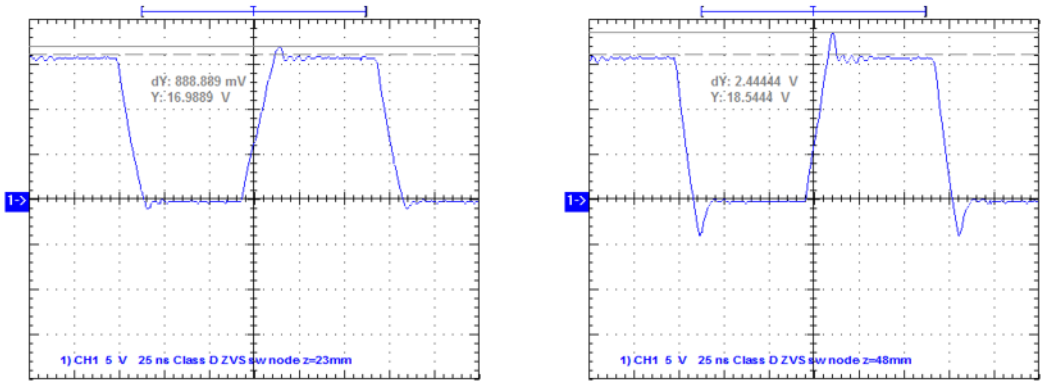

Figure 54 Coil distance variation in switch node waveform.

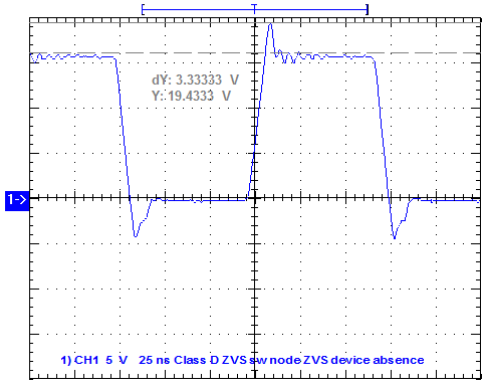

Figure 55 Receiver removed, z = ∞.

Above fig.55 shows switch node waveform overshoots heavily when device coil is absent. There is risk that peak voltage during overshoot exceeds the switching device voltage rating. Therefore it is important to study what are impacts of loading condition variations to switch node waveform. It is also notable in fig.55 that switch node is going negative for rather long time, this can lead into high reverse conducting loss in the switching device. Effect of foreign metal object on switch node waveform is very small. It can be compared to effect that comes from small R_{DCload} variation.

Performance test set-up

All measurements were accomplished in two different coil distance at $z = 23mm$ and $z = 48mm$. The coil set used in testing was A4WP compliant Class-3 source coil and Gategory-3 receiver coil shown in fig.56. During all measurements coils were placed concentrically in parallel alignment. The main measured parameter was the power transfer efficiency that was measured as DC power out divided by DC power supplied to the amplifier, excluding gate driver and other sub-circuit power consumption. In the forefront of fig.56 is seen adjustable capacitor that was used to tune matching between amplifier and coil set.

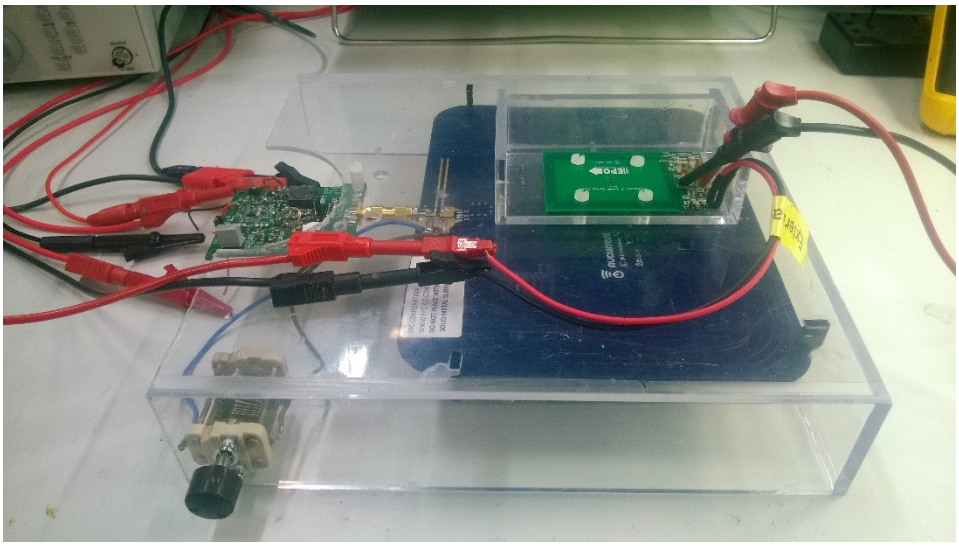

Figure 56 Mechanical assembly of measurement set-up.

Three different measurement were performed:

1. Load variation

The idea was to keep supply voltage fixed and find out the effect of load variation to the system performance. DC load resistance R_{DCload} was varied in range of 10 - 60Ω and power transfer efficiency were measured. The result of this test was to see which loading condition i.e. R_{DCload} value gives the best efficiency and that value was used in following testing procedure.

2. Peak performance

The peak performance test was based on the optimal loading condition in order to find out maximal power transfer efficiency that system could achieve. The supply voltage was varied while R_{DCload} was kept constant. The power transfer efficiency was measured as function of output power.

3. Regulated output voltage

While R_{DCload} was varied in discrete steps the supply voltage was put on such value that load side voltage was kept constant through the test. This kind of arrangement emulates system with regulated output voltage system with feedback loop. The power transfer efficiency was written down in function of R_{DCload}.

Fig. 57 and 58 below show the measurement setup during above tests. Power transfer efficiency were measured as DC power received in PRU divided by DC power supplied to the PTU.

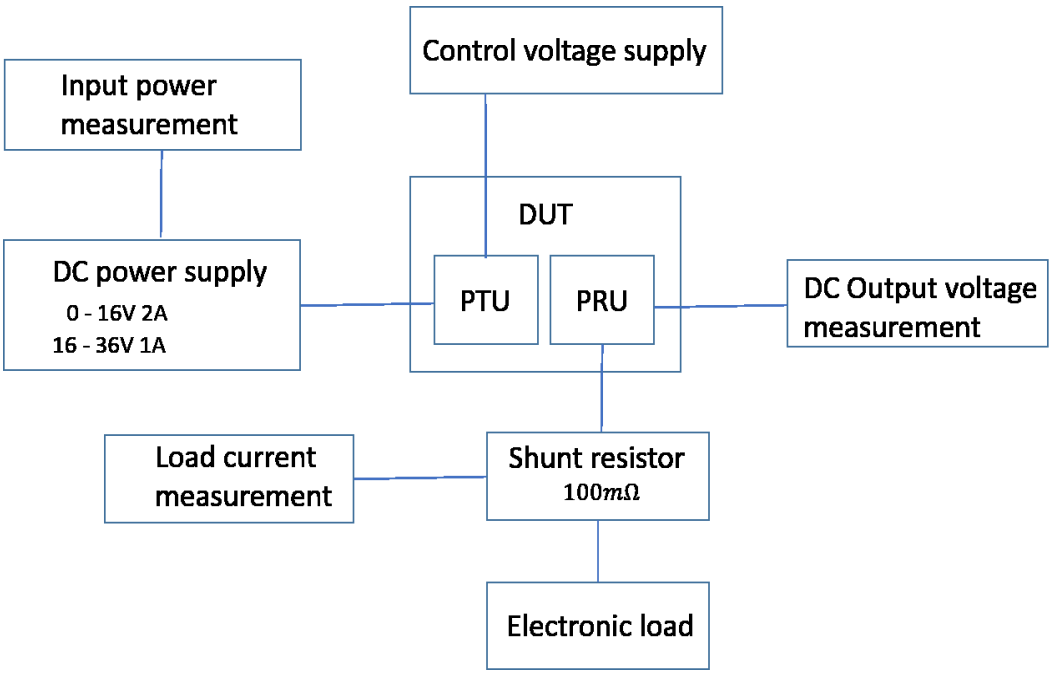

Figure 57 Power transfer efficiency measurement setup.

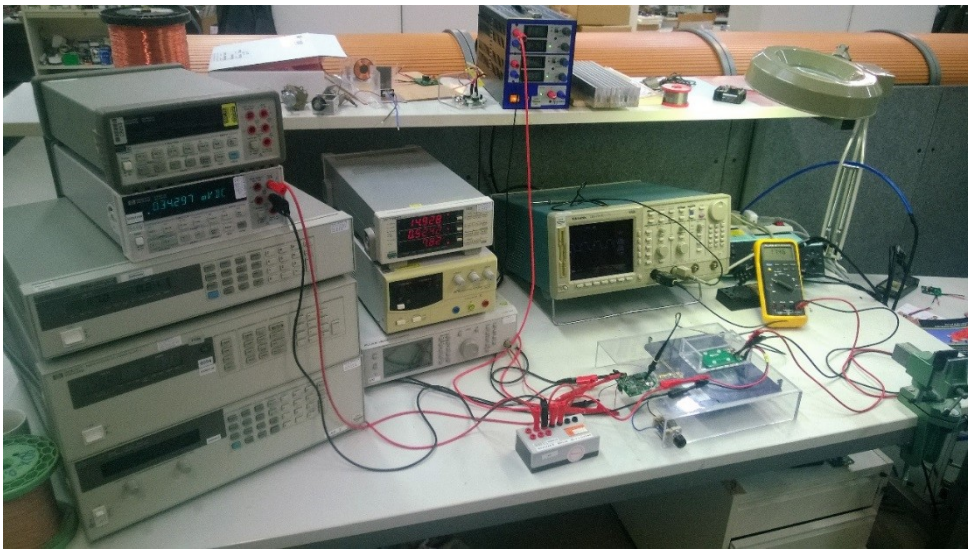

Figure 58 Measurement set-up in laboratory.

Performance test results

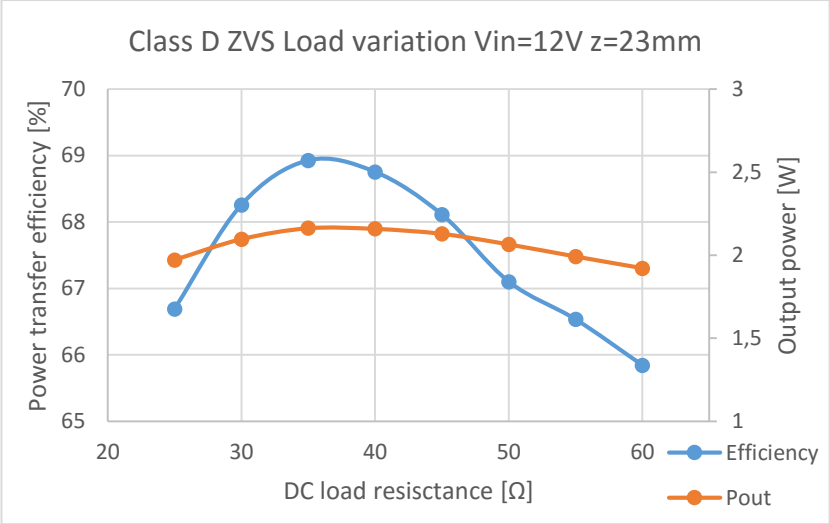

Figure 59 Class D ZVS Load variation V_{in}=12V z=23mm

Table 4 DUT in fig.59.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
12	0,24-0,26	2,92-3,14	7,13-10,9	0,28-0,18	1,92-2,16	25-60

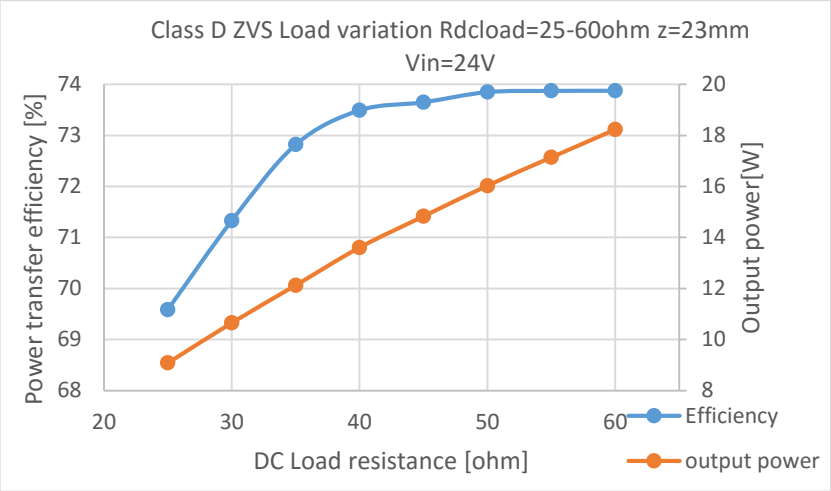

Figure 60 Class D ZVS Load variation R_{DCload}=25-60Ω z=23mm V_{in}=24V

Table 5 DUT in fig.60.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
24	0,54-1,03	13,1-24,7	15,2-33,2	0,60-0,55	9,09-18,2	25-60

Load variation test (fig.59 and 60) at coil distance z=23mm gives for optimal loading condition $R_{DCload} = 50\Omega$. During the test used supply voltage $V_{in} = 24V$ was selected in the basis that it gave the highest efficiency value. Remarkable in fig.60 is also how output power is increasing quite linearly with respect to R_{DCload}. As we remember coil set reflected impedance real value R_{load} is inversely proportional to the dc load resistance R_{DCload}. That explains the output power capability improving while R_{DCload} is increasing. At $R_{DCload} = 60\Omega$ DC power supply current limit was reached and test was stopped.

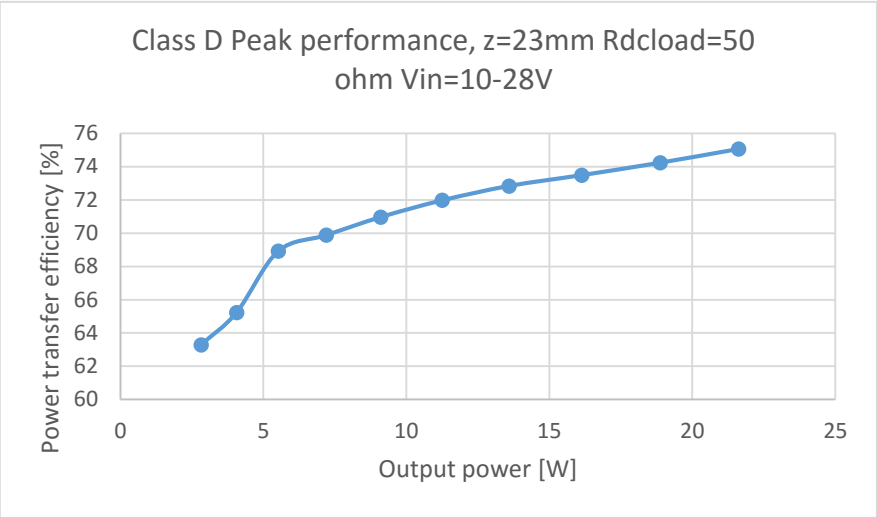

Figure 61 Class D Peak performance, z=23mm R_{DCload}=50 Ω V_{in}=10-28V.

Table 6 DUT in fig.61.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
10,0-27,9	0,45-1,03	4,46-28,8	12,0-33,1	0,24-0,65	2,82-21,6	50

As it is typical for many power conversion systems, the efficiency is improving while the output power is growing. The highest measured efficiency in fig.61 for Class D ZVS was 75%.

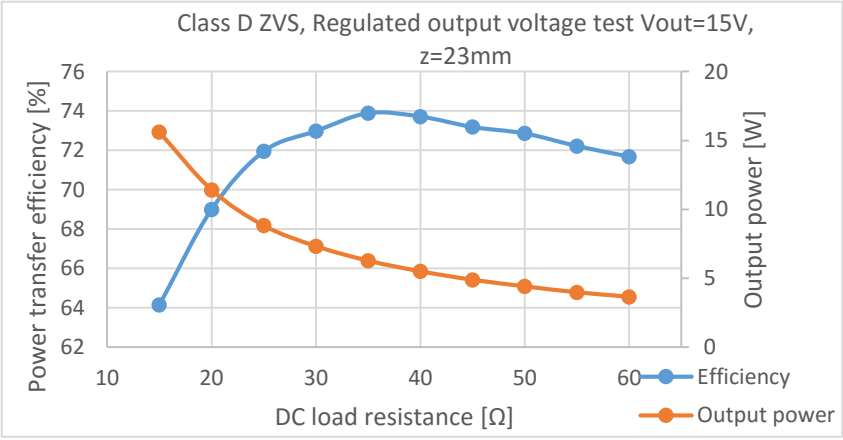

Figure 62 Class D ZVS, Regulated output voltage V_{out}=15V, z=23mm

Table 7 DUT in fig.62.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
30,0-13,0	0,81-0,40	24,3-5,12	15	1,04-0,24	15,6-3,67	15-60

Regulated output voltage test for Class D ZVS at $z = 23mm$ distance showed in fig.62 that optimal operation point around $R_{DCload} = 35\Omega$. As we can see the optimal operation point is shifted down from value we got in load variation test. This happens because output power is forced into specific point with output voltage regulation. Most likely, for same reason output power is also decreasing as DC load resistance is increasing against its natural characteristics operation.

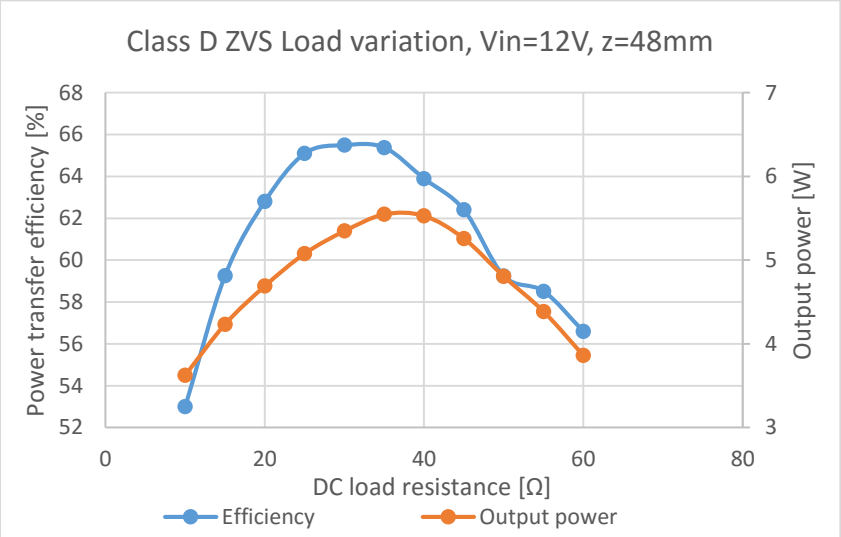

Figure 63 Class D ZVS Load variation, V_{in}=12V, z=48mm

Table 8 DUT in fig.63.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
12	0,57-0,72	6,84-8,65	5,89-15,5	0,62-0,25	3,63-5,55	10-60

Load variation test in fig. 63 shows clearly the optimal DC load resistance. Below the optimal DC load resistance, load seen by amplifier becomes more capacitive and it appears as a shift in resonance frequency of coil set. Above the optimal DC load resistance, load seen by amplifier becomes more inductive, which also change the resonance frequency and decreases power transfer efficiency of the system.

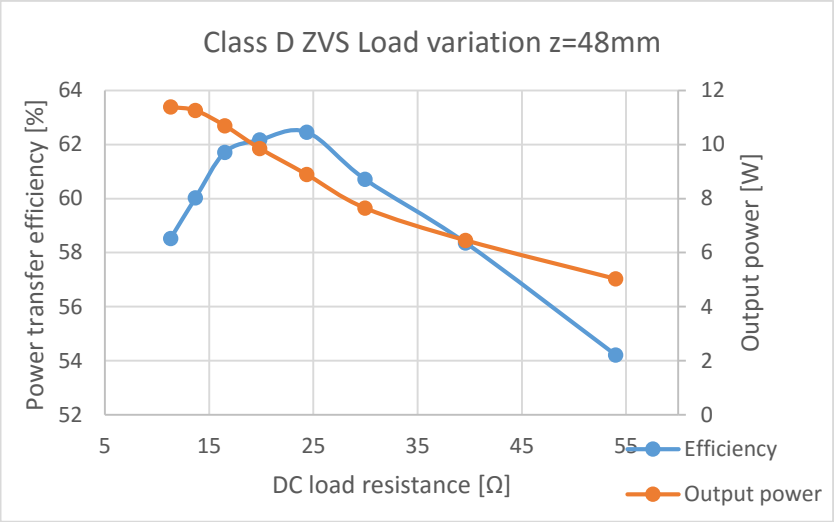

Figure 64 Class D ZVS Load variation z=48mm.

Table 9 DUT in fig.64.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
19	1,03-0,34	19,5-7,70	11,4-17,3	1,00-0,21	11,4-5,03	10-55

Load variation test was carried out with $V_{in} = 19V$ in fig.64. Higher the input voltage V_{in} is used in load variation test that lower the optimal DC load resistance tends to move. Load variation test with Vin=24V could not be carried out because DC power supply and same time A4WP class 3 coil nominal current limit was reached before maximum efficiency was achieved. Moreover, it seems that when distance between coils increases the optimal DC load resistance point tends to get lower.

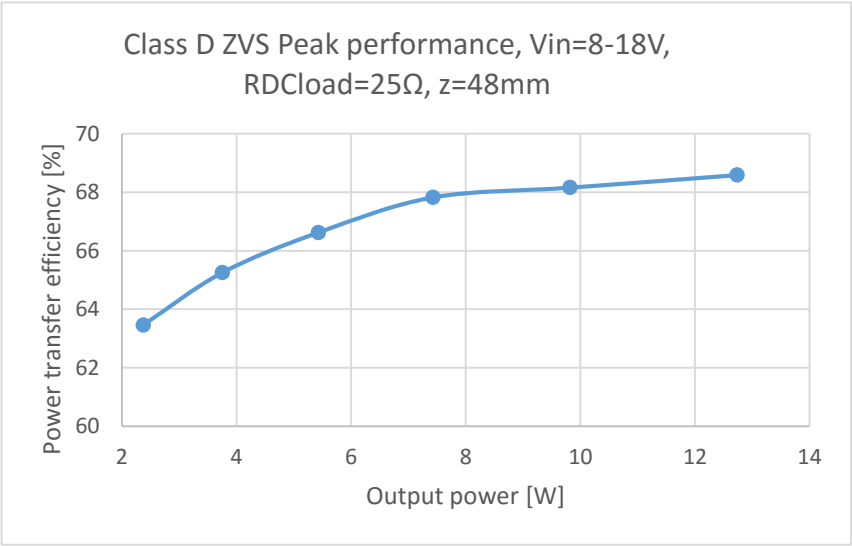

Figure 65 Class D ZVS Peak performance, V_{in}=8-18V, R_{DCload}=25Ω, z=48mm.

Table 10 DUT in fig. 65

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
8-18	0,47-1,03	3,74-18,6	7,81-18,1	0,30-0,70	2,37-12,7	25

The peak performance test at $z = 48mm$ in fig.65 shows what was expected. The efficiency is improving while the output power is growing. Increasing the coil distance from 23mm to the 48mm decreases the efficiency about 7%.

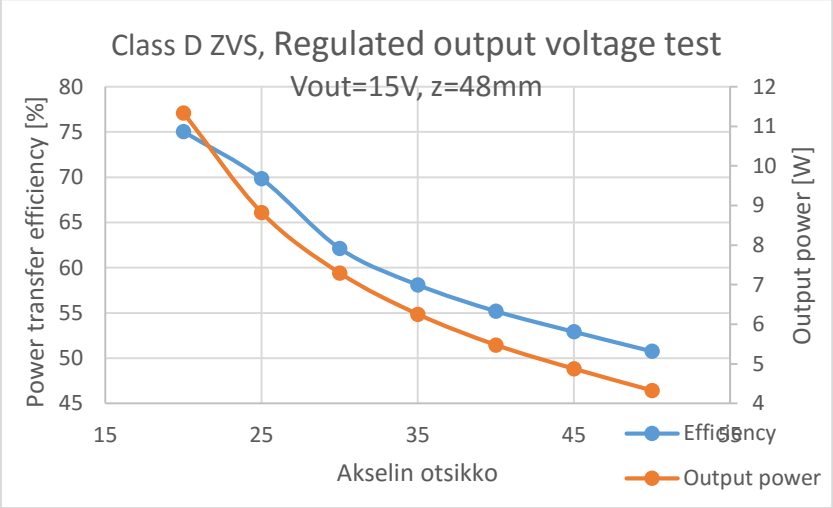

Figure 66 Class D ZVS, Load regulation V_{out}=15V, z=48mm.

Table 11 DUT in fig. 66

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
17,7-12,7	1,01-0,57	15,1-8,53	15	0,76-0,29	11,3-4,33	20-50

Also the load regulation test at $z = 48mm$ supports the notion that optimal DC load resistance moves down when coil distance is increased fig.66. Again DC power supply and same time A4WP class 3 coil nominal current limit was reached before optimal DC load resistance attained.

Thermal performance

Thermal performance of Class D ZVS power amplifier was studied in three different power levels. First two cases under testing were chosen to have power levels that could be relevant in real Class 3 wireless power transfer system. Loading condition were chosen to give maximal efficiency on that power level. The last case under thermal testing represents maximum power condition where 26W power is delivered into load. During measurements amplifier was operating at 23℃ ambient temperature without heat sinks or forced air cooling. The main concern in this thermal performance evaluation is switching device and its driver circuit temperature. In table 12 are electrical characteristics of the chosen operation point for 12W thermal performance measurement.

Table 12 DUT in fig.67.

Source board			Device board				efficiency
V_{DD} [V]	I_{rms} [A]	P_{in} [W]	V_{DC} [V]	I_{DC} [A]	P_{out} [W]	R_{DCload} [Ω]	η [%]
22,4	0,54	12,2	16,5	0,54	8,84	30	72,7

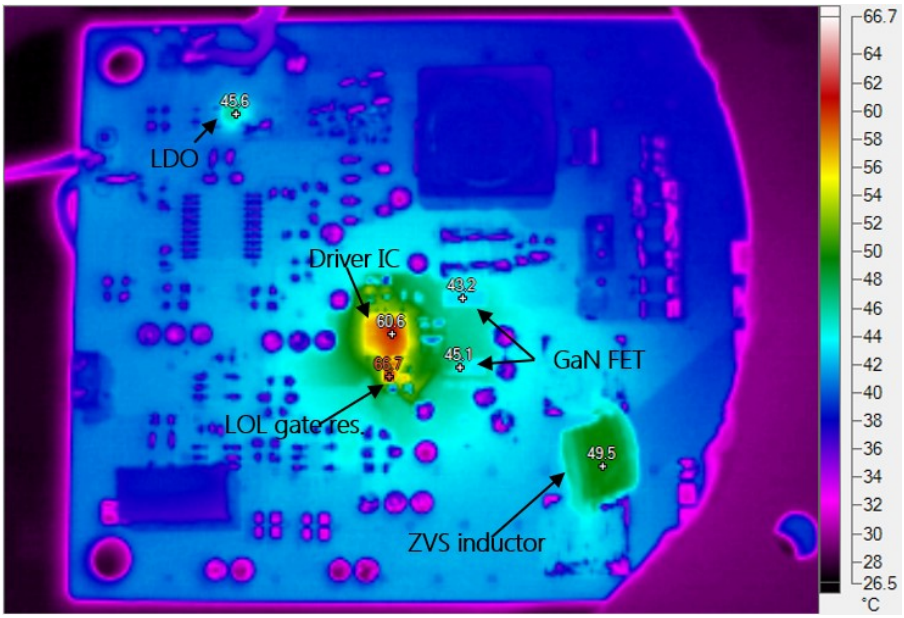

Figure 67 Thermal performance at 12W z=23mm.

Fig.67 shows that hottest component on the board is low-side gate pull-down resistor at 67℃ temperature. Second hottest component is gate driver-IC with 61℃ temperature. Datasheet [22] gives for maximum GaN FET junction temperature 150℃ and at this operation point junction temperature is not even close to the limit. At this power level both high-side and low-side switches runs at very low temperature 43℃ and 45℃ respectively. Other notable heat sources on board are ZVS air core inductor with almost 50℃ temperature and LDO regulator at the upper left corner with 46℃ temperature.

In table 13 are electrical characteristics of the chosen operation point for 18W thermal performance measurement.

Table 13 DUT in fig.68.

Source board			Device board				efficiency
V_{DD} [V]	I_{rms} [A]	P_{in} [W]	V_{DC} [V]	I_{DC} [A]	P_{out} [W]	R_{DCload} [Ω]	η [%]
26,9	0,68	18,4	20,5	0,67	13,7	30	74,3

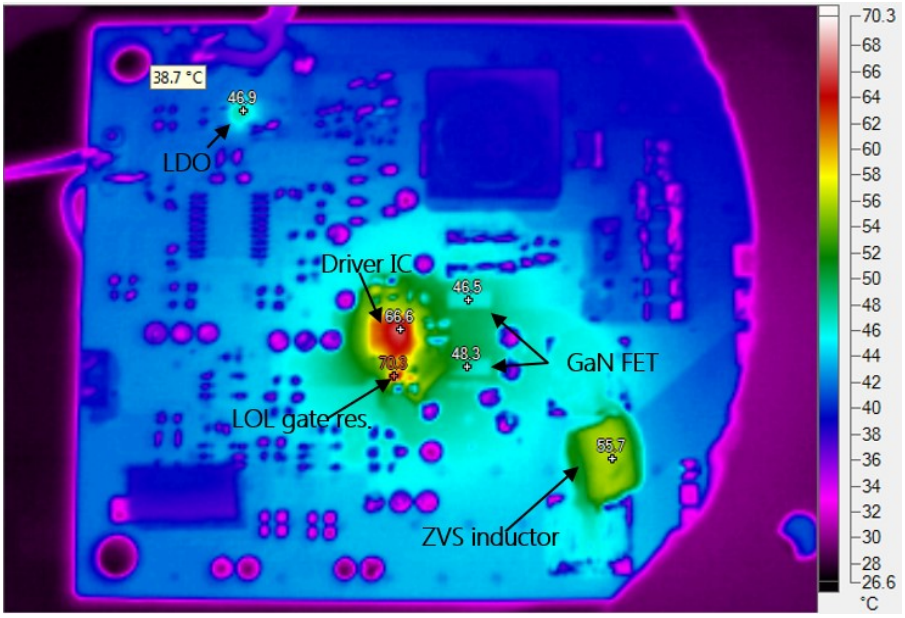

Figure 68 Thermal performance at 18W z=23mm.

Fig.68 shows that increasing power level 50% raises gate driver-IC temperature no more than 5℃ and switching device temperature little more than 3℃. All temperatures on board are in acceptable limits.

In table 14 are electrical characteristics of the chosen operation point for 26W thermal performance measurement.

Table 14 DUT in fig.69.

Source board			Device board				efficiency
V_{DD} [V]	I_{rms} [A]	P_{in} [W]	V_{DC} [V]	I_{DC} [A]	P_{out} [W]	R_{DCload} [Ω]	η [%]
31,9	0,84	26,9	25,0	0,82	20,4	30	75,8

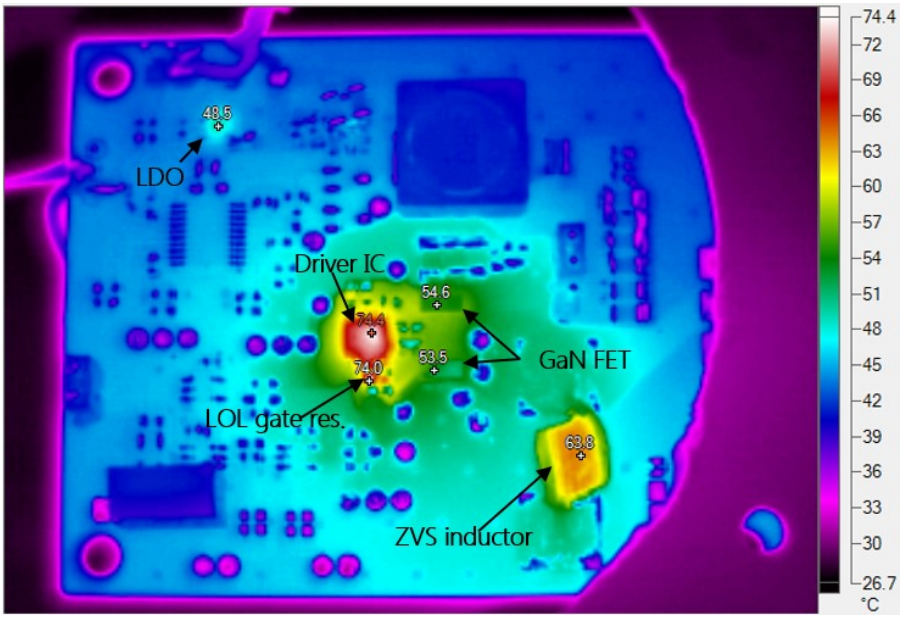

Figure 69 Thermal performance at 26W z=23mm.

Last fig.69 shows board temperatures at 26W input power. Still all temperatures are well below safety limits. Low switching device temperatures delights because it is indication of correctly tuned ZVS operation. Main loss sources are then gate driver-IC and ZVS air core inductor.

All these thermal measurements were done in open space at 23℃ ambient temperature. Closing the amplifier board into housing for sure raises ambient temperature and supposedly at power levels higher than 30W over heating might be an issue. But power levels that belong to A4WP Class 3 specification no heat sinks or forced air cooling should be needed even with tightly closed housings. For sure commercial products will be equipped with overheating protection circuits.

EMI measurements

Conducted EMI measurement performed was compliant with EN55022 standard. According to the standard measurement was completed in 150 kHz – 30 MHz frequency range.

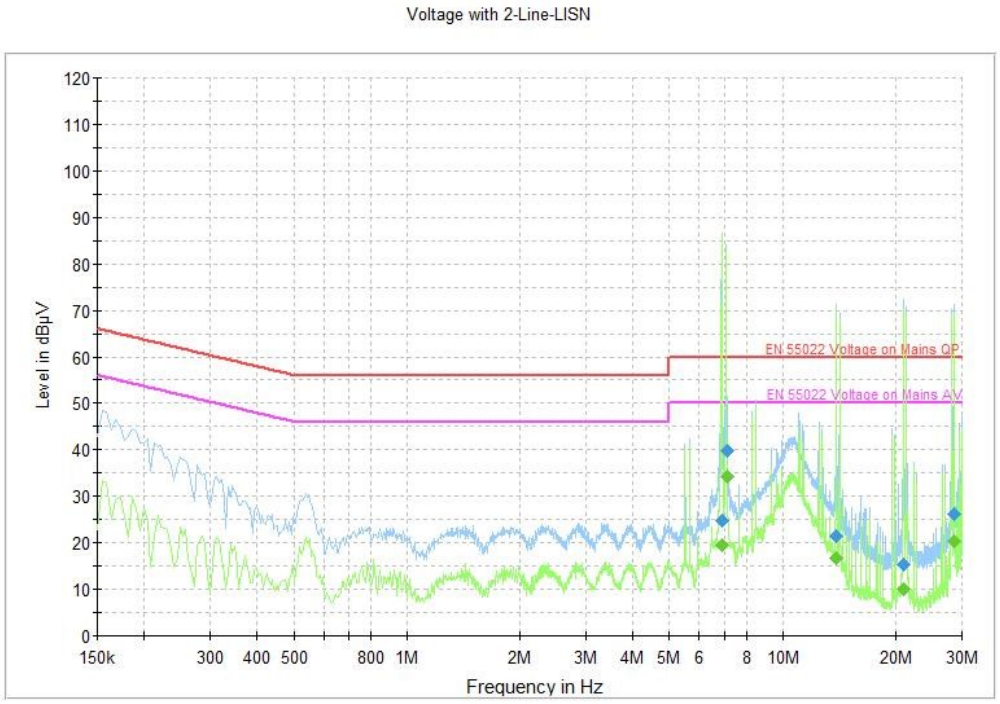

Figure 70 Conducted EMI measurement for Class D ZVS.

Measurements for conducted EMI (fig.70) showed pretty much that was expected. In advance, the switch node waveform was known to be very close to square wave and therefore significant odd harmonics of switching frequency was expected to appear at frequency content of conducted EMI measurement. Surprisingly there was also high magnitude frequency content close to second order harmonic of fundamental frequency, which should not appearance with ideal square wave. Most probably the second order harmonic content was originated by ZVS function that shapes the switch node square wave, it slows down switch node waveform rise and fall times and effectively modifies waveform square wave towards trapezoidal form.

5.4 Class E

Block diagram in fig.71 shows main components that needed to be designed. The full circuit schematic, PWB layout and BOM of Class E design are shown respectively in Appendix D, E and F.

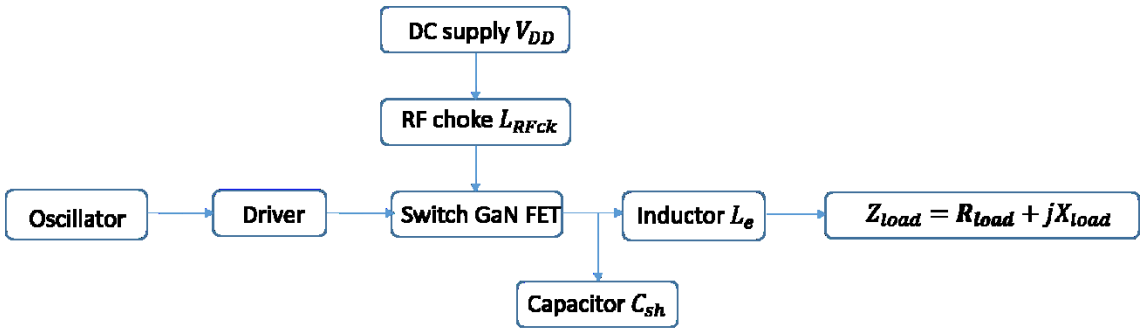

Figure 71 Class E block diagram.

Design specifications and critical component selection

Design specifications for Class E amplifier were very much the same as they were for Class D ZVS amplifier. Same A4WP compliant coil set was intended to use in testing with Class E amplifier and same 12W was the target output power.
To achieve the best performance of Class E amplifier, knowing the intended resistance value R_{load} of reflected load impedance Z_{load} would be very advantageous. In the beginning of the design process there were no idea about the value of the reflected load impedance Z_{load} resistive part R_{load}. After some pre-calculations the operation voltage V_{DD} was chosen to be 12V. From design equation (23) that was given in [16] R_{load} was derived and by substituting there $V_{DD} = 12V$ and $P_{load} = 12W$. Like in case with Class D ZVS, values V_{DD} and R_{load} are design specifications and they are used in passive component calculations.

$$V_{DD} = \sqrt{\frac{R_{load} * P_{load} * (\pi^2 + 4)}{8}} \tag{23}$$

$$R_{load} = \frac{8}{\pi^2 + 4} * \frac{V_{DD}^2}{P_{load}} = \frac{8}{\pi^2 + 4} * \frac{12^2 V}{12W} = 6{,}92\Omega$$

Switching device selection

From the theory of Class E amplifier it was known that in optimal operation point drain-to-source voltage $V_{DS} = 3{,}56 * V_{DD}$. However, in wireless power transfer can be very high load and coupling variations, which are de-tuning the amplifier. It is not unusual to see even $7 * V_{DD}$ drain-to-source peak voltages with Class E amplifier in certain loading conditions [16]. To have an option use amplifier with 24V supply voltage switching device with 200V maximum voltage rate was chosen.

The output capacitance C_{oss} value is determinant when selecting switching device for Class E amplifier. Depending on R_{load} value C_{oss} can be too large and the design is impossible get tuned. Then new switching device with lower C_{oss} must be selected or

R_{load} need to be decreased. Later calculations for load network passive components high lights more importance of C_{oss} value.

Other selection criteria were enough high current capability and small $R_{DS,on}$ value. Knowing that Class E amplifier is operating in normal condition in ZVS mode it would be justified to choose as small $R_{DS,on}$ value as possible in order to achieve small conducting losses. Table 15 shows options for Class E design in EPC product catalog.

Table 15 Selection table for Class E switching device. Source: www.epc-co.com

Part Number	Configuration	V_{DS}	Max V_{GS}	Max $R_{DS(ON)}$ (mΩ) @5V_{GS}	Q_G typ (nC)	Q_{GS} typ (nC)	Q_{GD} typ (nC)	Q_{OSS} typ (nC)	Q_{RR} (nC)	C_{ISS} (pF)	C_{OSS} (pF)	C_{RSS} (pF)	I_D (A)	Pulsed I_D (A)	Max T_J (°C)	LGA Package (mm)	Half-Bridge Development Board
EPC2110	Dual, Common Source	120	6	60	0.8	0.25	0.19	4.9	0	80	50	0.75	3.4	20	150	1.35 x 1.35	N/A
EPC2033	Single	150	6	7	10	3.5	1.7	66	0	1140	580	8	31	260	150	4.6 x 2.6	EPC9047
EPC2018	Single	150	6	25	5.0	1.3	1.7	40	0	480	270	9.2	12	60	125	3.6 x 1.6	N/A
EPC2034	Single	200	6	10	8.5	2.6	1.4	80	0	940	530	5	31	140	150	4.6 x 2.6	N/A
EPC2010C	Single	200	6	25	3.7	1.3	0.7	40	0	380	240	1.8	22	90	150	3.6 x 1.6	EPC9003C
EPC2010	Single	200	6	25	5.0	1.3	1.7	40	0	480	270	9.2	12	60	125	3.6 x 1.6	EPC9003
EPC2019	Single	200	6	50	1.8	0.60	0.35	18	0	230	110	0.7	8.5	42	150	2.7 x 0.95	EPC9014
EPC2012C	Single	200	6	100	1.0	0.30	0.20	10	0	100	64	0.4	5	22	150	1.7 x 0.9	EPC9004C
EPC2012	Single	200	6	100	1.5	0.33	0.57	11	0	128	73	3.3	3	15	125	1.7 x 0.9	EPC9004
EPC2025	Single	300	6	150	1.8	0.72	0.32	22	0	200	46	0.1	4	20	150	1.95 x 1.95	EPC9042

As Class E amplifier operates effectively in ZVS mode when tuned optimally, the same FOM expression that were used with Class D ZVS can be used also here to compare different devices. In FOM_{ZVS} expression $R_{DS,on}$ unit is expected to be $m\Omega$ $Q_{G,GD}$ unit nC.

$$FOM_{ZVS} = R_{DS,on} * (\mathrm{Q_G} - \mathrm{Q_{GD}})$$

EPC2010: $FOM_{ZVS} = 25 * (5{,}0 - 1{,}7) = 83$

EPC2034: $FOM_{ZVS} = 10 * (8{,}5 - 1{,}4) = 71$

Above calculation show that EPC2034 would be optimal choice, still EPC2010 was selected because it has lower C_{OSS} value which is important in Class E load network design. To make comparison with MOSFET, FOM_{ZVS} was calculated for Infineon OptiMOS™ with comparable electrical characteristic in table 16. Infineon OptiMOS™ is known state-of-art switching power MOSFET product.

Table 16 Comparable MOSFET devices.

Part	V_{DS} [V]	$R_{DS,on}$ $[m\Omega]$	$\mathrm{Q_G}$ $[nC]$	$\mathrm{Q_{GD}}$ $[nC]$	C_{oss} $[pF]$	I_D [A]	Package [mm]
BSC320N20NS3	200	32	22	3,0	180	36	5,0x6,0
BSZ240N12NS3	120	21	20	5	230	37	5,0x6,0

BSC320N20NS3: $FOM_{ZVS} = 32 * (22 - 3{,}0) = 608$

BSZ240N12NS3: $FOM_{ZVS} = 21 * (20 - 5) = 315$

Even though above shown comparison is very simple, it seems that GaN FET superior switching characteristics against MOSFET is more evident with higher V_{DS} rated devises.

Load network passive components

In Class E load network there is three components that need to be designed:

1. RF choke L_{RFck}
2. The shunt capacitor C_{sh}
3. The series inductor L_e

All the following calculations for load network components are based on design equations given by Rooij [16]. Originally these design equations are derived by Sokal & Sokal [15], but [16] gives them in more handy form for this purpose.

$$L_{RFck} > \frac{(\pi^2 + 4) * R_{load}}{4 * f_{sw}}$$

$$C_{OSSQ} = \frac{1}{V_{DSRMS}} * \int_0^{V_{DSRMS}} C_{OSS}(V_{DS}) * dv_{DS}$$

$$C_{sh} = \frac{4}{\pi^2 * (\pi^2 + 4) * f_{sw} * R_{load}} - C_{OSSQ}$$

$$L_e = \frac{\pi * (\pi^2 - 4) * R_{load}}{32 * \pi * f_{sw}}$$

The minimum value of RF choke in V_{DD} supply line is calculate below.

$$L_{RFck} > \frac{(\pi^2 + 4) * R_{load}}{4 * f_{sw}} = \frac{(\pi^2 + 4) * 15W}{4 * 6{,}78 * 10^6 Hz} = 8\mu H$$

Actual L_{RFck} value chosen was as high as 68µH. The higher L_{RFck} value means lower current ripple and possible more stable amplifier operation and improved EMI performance. As usual, there is trade-off between efficiency and EMI performance. A too high L_{RFck} will decrease the system total efficiency.

The total shunt capacitance includes switching device equivalent output capacitance C_{OSSQ} and external shunt capacitance C_{sh}.

$$C_{OSSQ} + C_{sh} = \frac{4}{\pi^2 * (\pi^2 + 4) * f_{sw} * R_{load}} = \frac{4}{\pi^2 * (\pi^2 + 4) * 6{,}78 * 10^6 Hz * 6{,}92\Omega} = 623pF$$

The peak switching device voltage in optimal design is

$$V_{DS} = 3{,}56 * V_{DD} = 3{,}56 * 12V = 42{,}72V.$$

To calculate C_{OSSQ} the RMS value of the peak device voltage is needed.

$$V_{DSRMS} = \frac{3{,}56 * 12V}{\sqrt{2}} = 30{,}21V$$

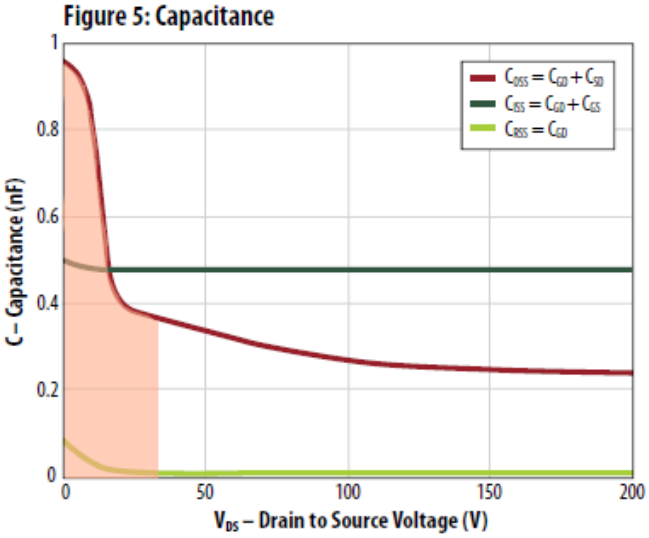

Figure 72 EPC2010 GaN FET parasitic capacitances from datasheet. [24]

The equivalent output capacitance C_{OSSQ} value is approximated as shaded area from fig.72 given in switching device datasheet [24].

$$C_{OSSQ} = \frac{1}{V_{DSRMS}} * \int_0^{V_{DSRMS}} C_{OSS}(V_{DS}) * dv_{DS}$$
$$= \frac{1}{30{,}21V} * (0{,}70nF * 20V + 0{,}38nF * 10{,}21V) = 592pF$$

The load network shunt capacitance $C_{sh} = 623pF - 592pF = 31pF$.
It is possible that calculated C_{OSSQ} value is larger than the total shunt capacitance. In such a case the design is impossible and new switching device must be selected with lower C_{oss} or R_{load} need to be decreased. The last component to calculate in load network is the series inductor L_e.

$$L_e = \frac{\pi * (\pi^2 - 4) * R_{load}}{32 * \pi * f_{sw}} = \frac{\pi * (\pi^2 - 4) * 6{,}92\Omega}{32 * \pi * 6{,}78 * 10^6 Hz} = 187nH$$

Oscillator

For Class E amplifier design a crystal oscillator was selected to form a control pulse for gate driver circuit. The particular oscillator type Epson SG-210 STF was selected because the supplier had them in stock at right frequency (6.78MHz) for this purpose. In addition to the correct frequency only requirement for oscillator was that it can drive gate driver circuit straight without any intermediate circuits like buffer-IC. Oscillator output is CMOS type so it is compatible with driver input that accepts both TTL and CMOS level input signals.

Driver requirements

Advantage of Class E amplifier is that only one active switching device is needed and a simple ground referenced low side gate driver is therefore needed. The driver-IC UCC27611DRVT was selected based on the recommendation of GaN FET manufacturer. UCC27611DRVT driver-IC has precisely controlled 5V gate drive voltage, which ensures that maximum 6V gate-to-source voltage of GaN FET is not exceeded. The splitted output of UCC27611DRVT allows optimal adjustment for the gate turn-on and off while gate resistances are chosen independently. The driver is also secured with UVLO action to prevent unstable operation of switching device. Moreover this particular driver IC pin out is optimized for EPC GaN FET footprint and therefore optimal layout design is easy to make.

5.5 Measurements for Class E

In fist part optimal Class E tuning is introduced and effect of load variation in ZVS operation is demonstrated. Second part of measurements is reserved for performance tests. Third part shows Class E amplifier thermal performance in three different power level while the last part is reserved for conducted EMI measurements. Fig.73 shows assembled Class E power amplifier testing board.

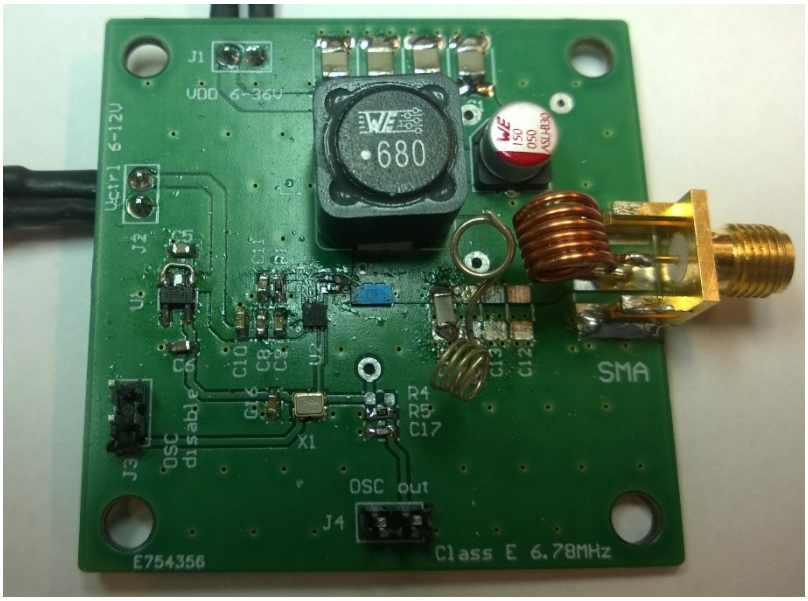

Figure 73 Assembled Class E testing PWB.

ZVS tuning

The tuning of the Class E amplifier was detected from switching device drain-to-source voltage. Adjustment in practice were performed by adjustable capacitor seen in fig.74. After tuning adjustable capacitor value was measured and replaced with equal discrete capacitor. Fig.75 shows optimally tuned Class E operating in ZVS mode.

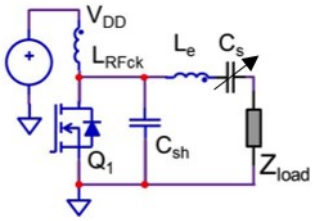

Figure 74 Class E ZVS tuning with adjustable capacitor. [16]

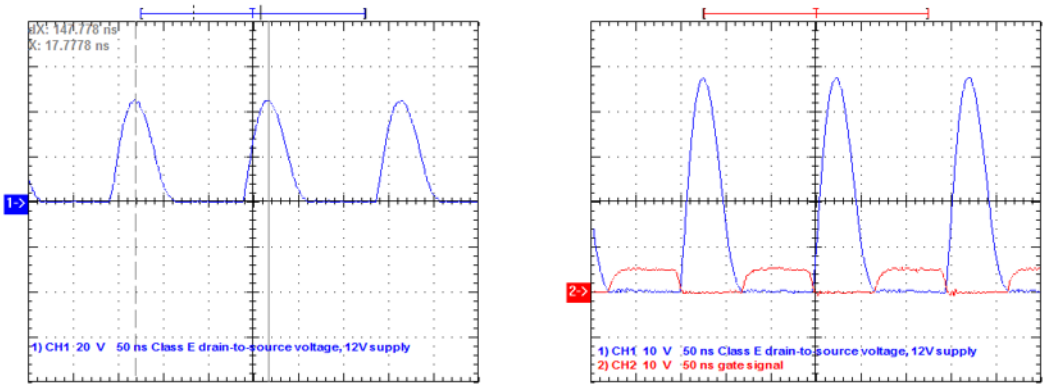

Figure 75 Left: In optimal tune $V_{DS} = 3{,}56 * V_{DD}$. Right: V_{DS} voltage wave form and gate signal.

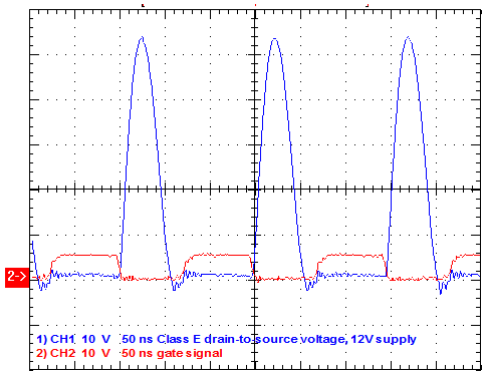

Figure 76 De-tuned ZVS action when R_{load} < design point

Fig.76 shows how V_{DS} looks like when $R_{load} < design\ point$. Design point refers here to optimal R_{load} that was used in component value calculations. Too small R_{load} value leads to condition where load tends to draw current too fast from the amplifier output, it is seen on fig.76 as a shorter pulse width. To compensate this too quick current flow, V_{DS}voltage gets therefore much higher than in optimal loading. Voltage V_{DS} can be

even $7 * V_{DD}$ so there need to be much room in switching device voltage rating to ensure safety operation in varying load conditions. This kind of operation condition leads to higher switching device voltage strain and device can turn into reverse conduction mode before gate voltage is getting high. Especially when operating with GaN FET, body diode conducting can lead high losses because of higher reverse conducting voltage when comparing to MOSFET.

In fig.77 left there is a typical V_{DS} waveforms when $R_{load} > design\ point$. Now load is unable to draw enough current from amplifier output before gate is switched high and ZVS operation condition is lost. Voltage over switching device when switch is turned on leads to C_{OSS} losses. Influence of too high R_{load} is seen more clearly in fig. 77 right. High frequency oscillating is seen in gate signal as well in drain-to-source voltage and voltage peak is lower than in optimal operating point. For sure EMI measurements are suffering from this kind of ringing waveforms. Optimal operating point can be found by trial and error method or using circuit simulator.

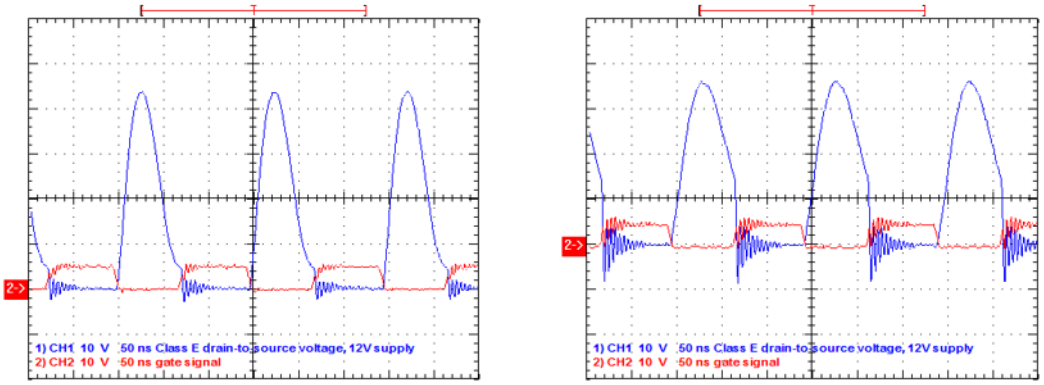

Figure 77 Typical V_DS waveform when R_{load} > design point.

Performance test results

All efficiency measurements here are DC power IN to DC power OUT excluding gate driver, oscillator and all other sub-circuit power consumption. Measurements are done in two different z-distances 23mm and 48mm. During all measurements TX coil and Rx coil were placed concentrically. Measurement data shown here were collected in same manner as it was done for Class D ZVS earlier.

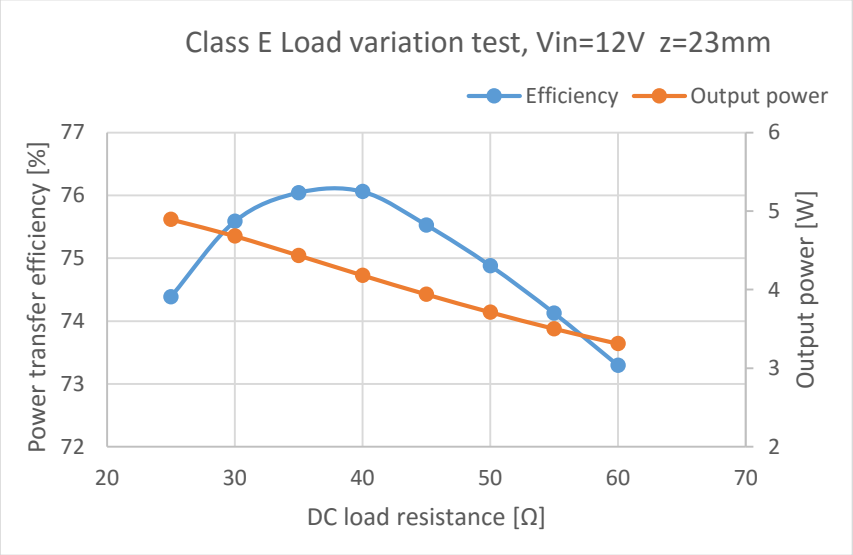

Figure 78 Class E Load variation test, V_{in}=12V $z = 23mm$

Table 17 DUT in fig.78.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
12	0,55-0,38	6,58-4,52	11,2-14,3	0,44-0,23	4,89-3,31	25-60

Load variation test at coil distance $z = 23mm$ were accomplished with two different supply voltage $V_{in} = 12V$ (fig.85) and $V_{in} = 24V$ (fig.78). Both experiments gave almost equal value for optimal loading condition $R_{DCload} = 35\Omega$.

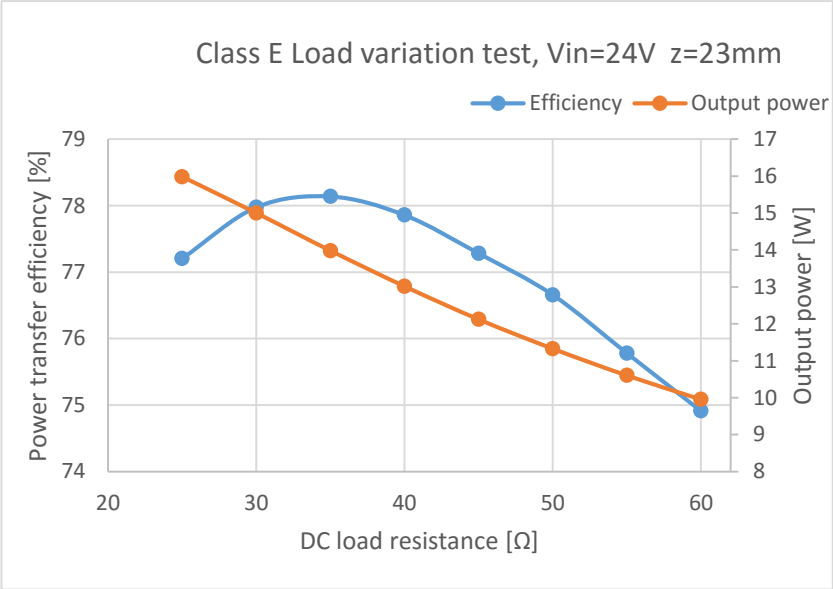

Figure 79 Class E Load variation test, V_{in}=24V z=23mm

Table 18 DUT in fig.79.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
24	0,86-0,55	20,7-13,3	20,2-24,7	0,79-0,40	16,0-10,0	25-60

When Class E type WPT system is operating below the optimal DC load resistance, efficiency is decreasing exponentially. Too low DC load resistance leads to condition where reflected impedance's real part R_{load} is above the design point and further leads to mess the correct ZVS operation. In fig.79 there is shown waveform of switching device drain-to-source voltage in such condition. C_{OSS} -related losses are increasing dramatically when there is voltage across drain-to-source when device is turned on. In addition to that coil impedance becomes more inductive [16].

If Class E type WPT system is operating above the optimal DC load resistance then the reflected impedance's real part R_{load} is below the design point. Linear decreasing seen in efficiency is then result of reverse conducting (GaN FET 'body diode conducting'). In chapter 9.1 ZVS tuning there is more detailed explanation for this loss mechanism. In addition to that coil impedance becomes more capacitive [16].

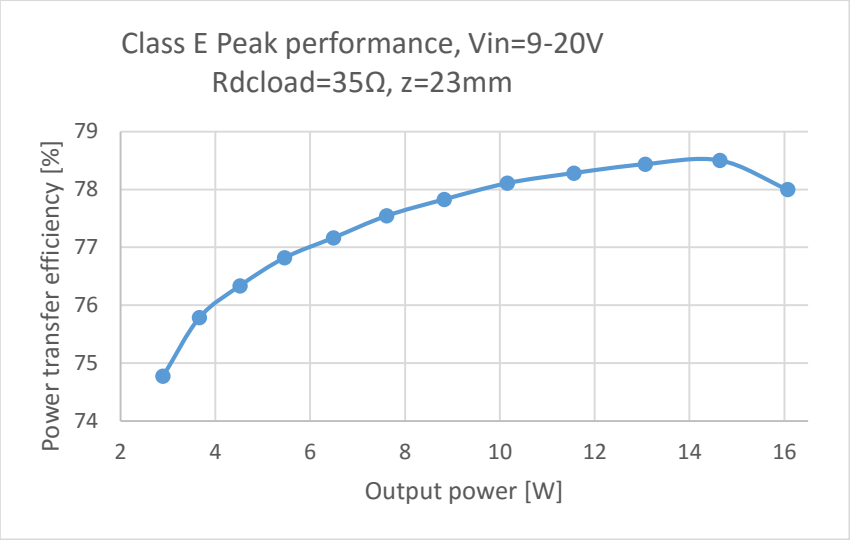

Figure 80 Class E Peak performance, V_{in}=9-20V R_{DCload}=35Ω, z=23mm

Table 19 DUT in fig.87.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
9,00-20,0	0,43-1,03	3,87-20,6	10,2-24,0	0,28-0,67	2,89-16,1	35

Fig.87 gives expected kind of result for peak performance of Class E type wireless power transfer system. The efficiency is improving while output power increases. Highest efficiency 78,5 % is achieved at the 14,6 W output power level and after that DC power supply current limit begin to restrict efficiency.

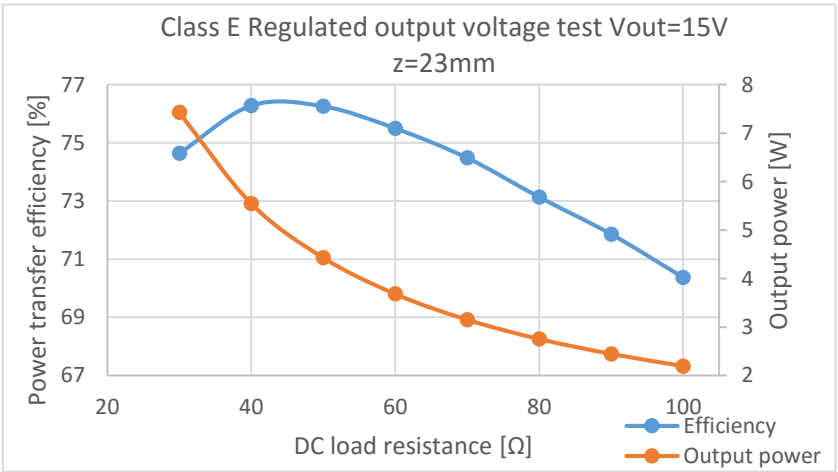

Figure 81 Class E Load regulation, V_{out}=15V z=23mm

Table 20 DUT in fig.81.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
12,7-9,6	0,78-0,32	9,95-3,12	15	0,50-0,15	7,43-2,19	30-60

Fig. 81 shows, like in case of Class D ZVS, how optimal DC load resistance is shifted due to the forced output power operation point. During load regulation test V_{in} was between range12.7V – 9.6V, meaning that most of the time DUT were operating under its intended operation voltage. That could be an explanation why optimal DC load resistance value is shifted to higher value even though the transition was thought to be shifted lower value.

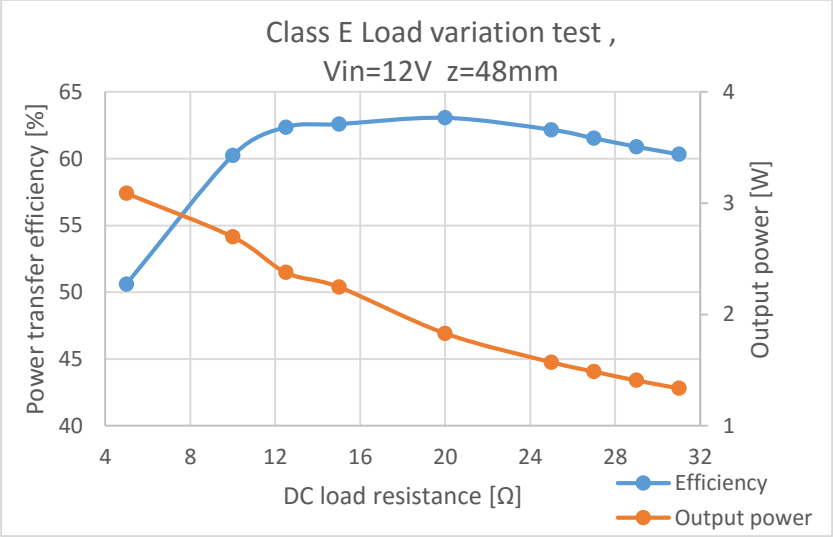

Figure 82 Class E Load variation test V_{in}=12V z=48mm

Table 21 DUT in fig.82.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
12	0,51-0,18	6,10-2,22	3,99-6,54	0,78-0,20	3,09-1,34	5,14-32,0

Fig.81 and 82 shows clearly fast degeneration of efficiency when DC load resistance is below optimal value. Class E amplifier seems to withstand more likely little bit too high DC load resistance values instead of too low DC load resistance values.

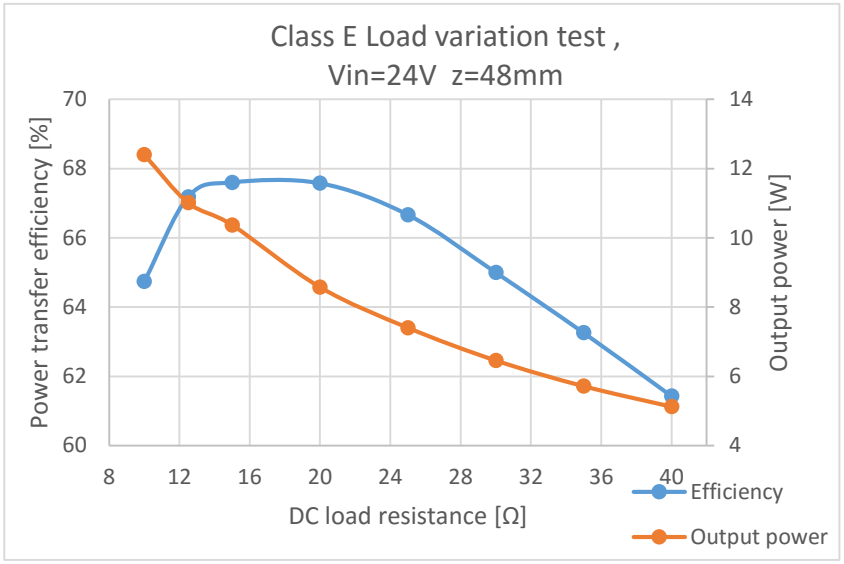

Figure 83 Class E Load variation test, V_{in}=24V z=48mm

Table 22 DUT in fig.83.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
24	0,80-0,35	19,2-8,34	11,0-14,5	1,12-0,35	12,4-5,12	10-40

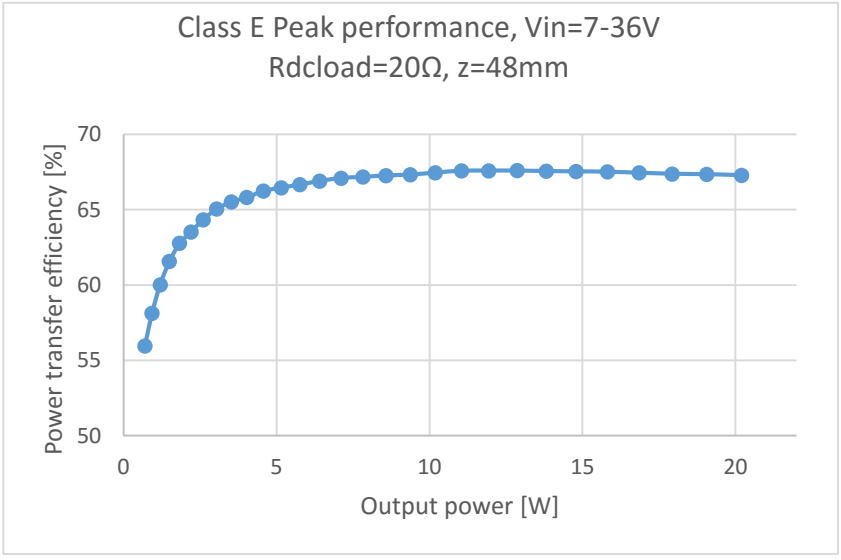

Figure 84 Class E Peak performance, V_{in}=7-36V R_{DCload}=20Ω, z=48mm

Table 23 DUT in fig. 84.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
8-36	0,16-0,83	1,25-30	3,73-20,1	0,19-1,00	0,70-20,2	20

Class E peak performance curve in fig.84 is in line with expectations. High power levels, with moderately good efficiency, were possible to deliver into load even in coil-to-coil distance of $z = 48mm$.

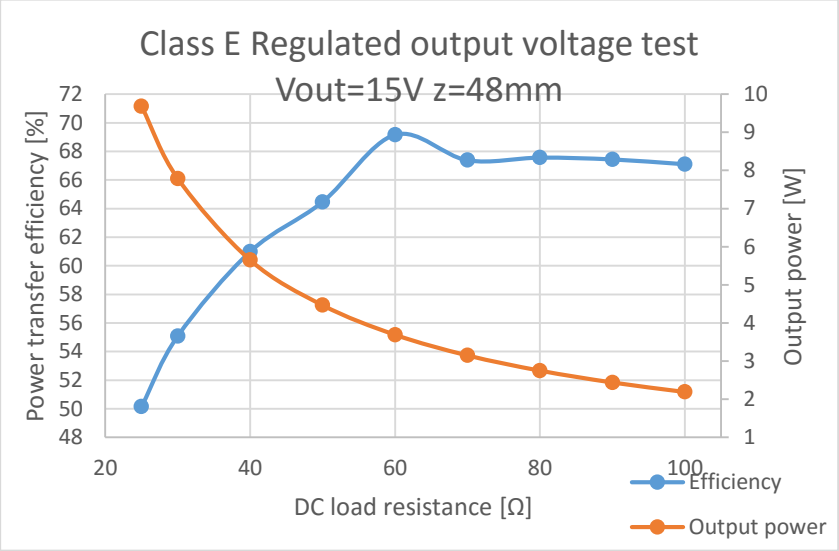

Figure 85 Class E Load regulation, V_{out}=15V z=48mm

Table 24 DUT in fig.85.

Source board			Device board			
V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
13,5-5,54	1,44-0,59	19,3-3,27	15	0,65-0,15	9,69-2,19	25-100

Fig.85 disclose the fact that Class E amplifier is able to keep relatively good efficiency with regulated load, power feed into load drops dramatically but losses in amplifier are not increasing despite the unfavorable load regulation.

Thermal performance

Thermal performance of Class E power amplifier was studied in three different operation points. First two cases under testing were chosen to have power level that could be relevant in real Class 3 wireless power transfer system. Loading condition were chosen to give maximal efficiency on that power level. The last case under thermal testing represents condition when maximum power is delivered into load with poor efficiency. During measurements amplifier was operating at 23℃ ambient temperature without heat sinks or forced air cooling. The main concern in this thermal performance evaluation is switching device and its driver circuit temperature. In table 25 are electrical characteristics of the chosen operation point for 12W thermal performance measurement.

Table 25 DUT in fig.86.

Source board			Device board				efficiency
V_{DD} [V]	I_{rms} [A]	P_{in} [W]	V_{DC} [V]	I_{DC} [A]	P_{out} [W]	R_{DCload} [Ω]	η [%]
12,0	0,97	11,6	17,9	0,50	9,0	35,0	77,3

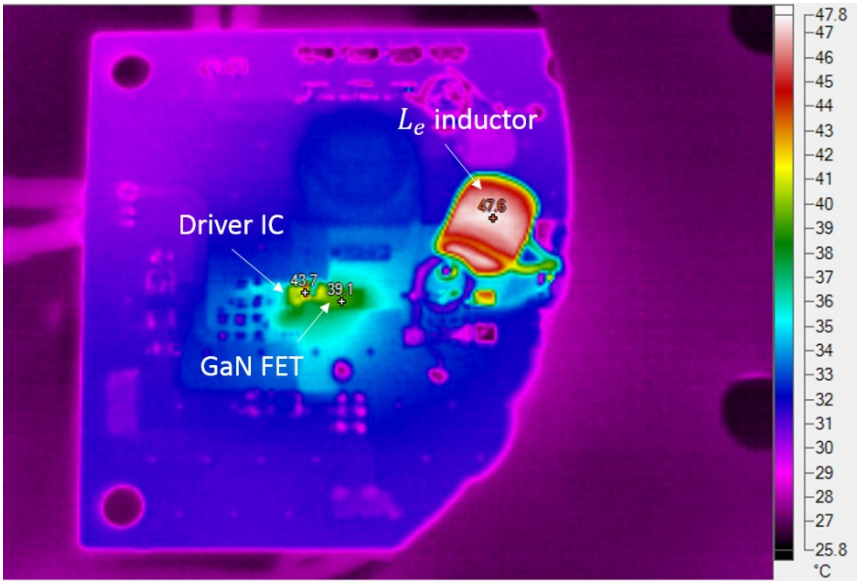

Figure 86 Class E thermal performance at 12W input power z=23mm.

Fig.86 shows critical temperatures on amplifier board at 12W input power. Obviously the hottest point on board is the air core inductor with about 50℃ temperature. Temperature of GaN FET is just below 40℃ and driver-IC temperature is less than 45℃. Hot spot seen below air core inductor is due to the tinned shining surface of the unused component pad, IR-camera can show irrelevant values from reflecting surfaces. In table 26 are electrical characteristics of the chosen operation point for 18W thermal performance measurement.

Table 26 DUT in fig.87.

Source board			Device board				efficiency
V_{DD} [V]	I_{rms} [A]	P_{in} [W]	V_{DC} [V]	I_{DC} [A]	P_{out} [W]	R_{DCload} [Ω]	η [%]
16,0	1,01	17,6	22,14	0,62	13,7	35	77,87

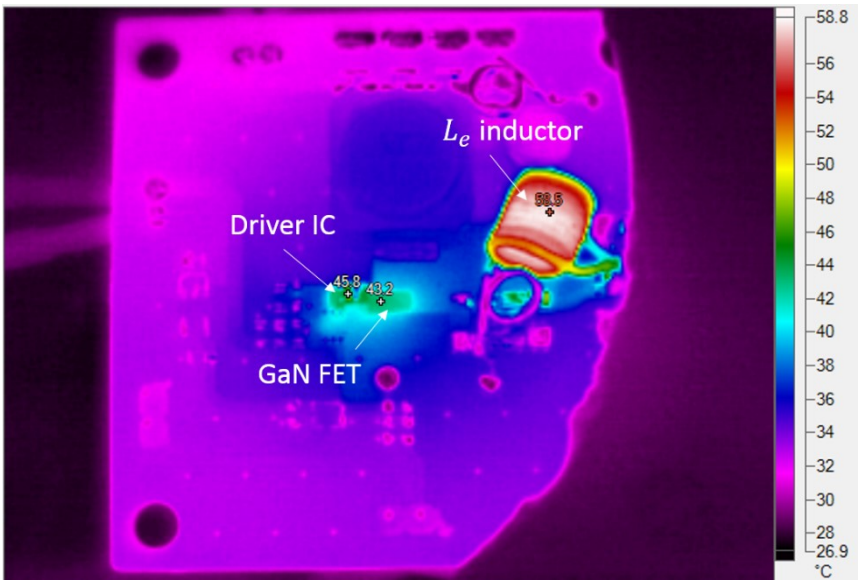

Figure 87 Class E thermal performance at 18 input power z=23mm.

Fig.87 shows critical temperatures on amplifier board at 18W. The hottest point on board is again the air core inductor with about 60℃ temperature. The surface temperature of GaN FET is around 43℃ and driver-IC temperature is little bit higher than 45℃. As we can see, increasing the power level 50% from 12W to 18W raises the temperature of critical components on board fairly moderately.

Last examination with Class E thermal performance was studied as worst case condition. Power level was chosen to be high while at the same time switching device voltage strain was very close to its maximum value. In addition, loading condition were selected to be such that power transfer efficiency were intentionally poor. In table 27 are electrical characteristics of the chosen operation point for 26W thermal performance measurement.

Table 27 DUT in fig.88.

Source board			Device board				efficiency
V_{DD} [V]	I_{rms} [A]	P_{in} [W]	V_{DC} [V]	I_{DC} [A]	P_{out} [W]	R_{DCload} [Ω]	η [%]
40,0	0,65	25,9	24,2	0,67	16,2	35	67,3

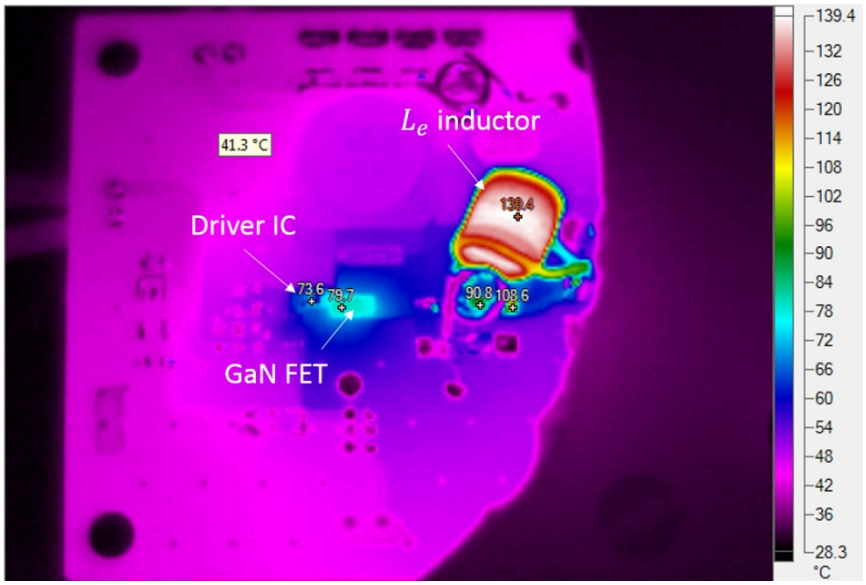

Figure 88 Worst case thermal performance at 26W input power and poor efficiency z=48mm.

From fig.88 can be seen the importance of keeping amplifier in-tune. Temperatures in board are remarkably higher than in two earlier case. Switching device temperature is almost twice that it was in earlier cases, even though current through switching device is now lower. Air core inductor reaches even 140℃ which is unacceptable high. Detuning the amplifier increases losses in circuit board into unacceptable level. Though all components can stand the temperatures seen in this examination, efficiency value of 67.3% is too low to accept.

As a summary, thermal performance examinations showed that it is possible to deliver A4WP Class 3 specified power level into source coil without using heat sink or forced air cooling in the board. By keeping amplifier tuned i.e. in optimal loading condition, efficiency stays high and temperatures in acceptable level.

EMI measurements

The conducted emission measurement for Class E WPT system fig.89 shows the unfortunate fact that Class E topology produces both even and odd order harmonics. Even-order harmonics are originated from dual resonant frequency structure of Class E topology, they can be very troublesome as they have asymmetrical impact on fundamental frequency and can cause power fluctuations [16].

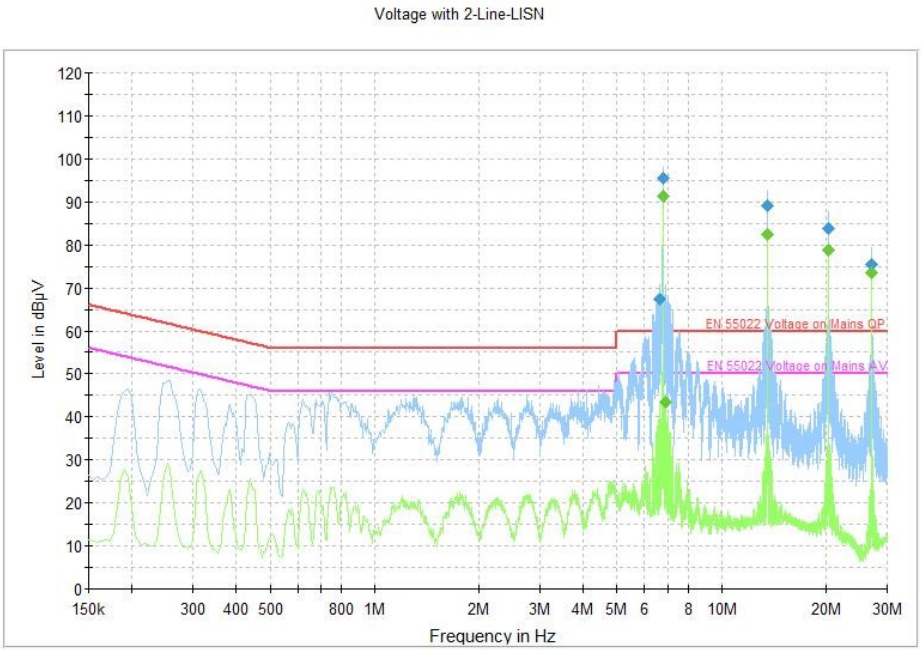

Figure 89 Conducted emission measurement for Class E WPT

To verify conducted emission measurement distortion in supply voltage was measured with oscilloscope. Strong ripple component was found at 6.78MHz switching frequency and also clearly visible ripple component at one decade higher about 70MHz in fig.90. Amplitude of voltage ripple at 6.78MHz is measured as high as 73mV. Approximation about the level that is measured in conducted EMI measurements. In the worst case measurements, actually as high noise level were measured as fig.89 verify.

$$20\log_{10}\left(\frac{73mV}{1\mu V}\right) = 97dB\mu$$

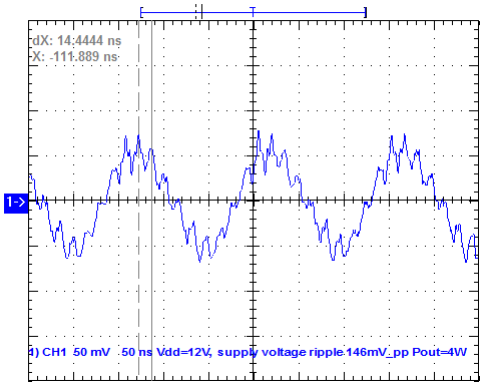

Figure 90 Distortion in supply voltage.

5.6 Topology comparison

In this chapter Class E and Class D ZVS main on-resonance performance test results are compared. This comparison is made from the same data that was collected for amplifiers individual performance tests earlier. At the end of the chapter feasibility of both amplifier topologies for wireless power transfer system are discussed.

There are several sources of error that can add uncertainty to the performance measurement and make topology comparison problematic. First of all, switching device selection affects significantly into performance of amplifier and you cannot be sure that optimal switching device is selected for both amplifier topologies in this work. It is possible that used coil-set is more suitable for other topology or matching is more successfully implemented with other topology. The different R_{DCload} value also may have an effect on matching result. This comparison also ignores the fact that operation power consumption, i.e. gate drive power and all sub circuits, is different between Class D ZVS and Class E.

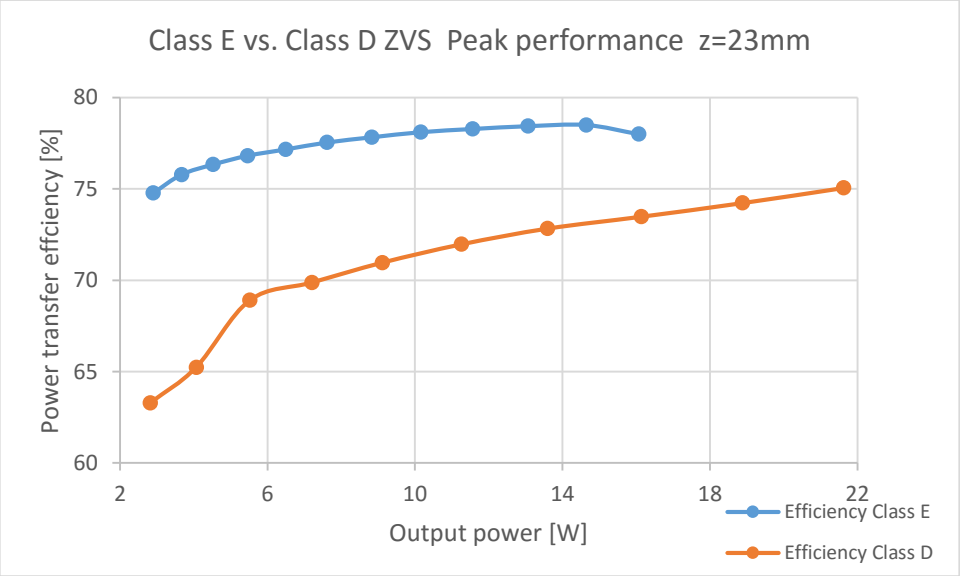

Figure 91 Class E vs. Class D ZVS Peak performance z=23mm.

The peak performance of both Class E and Class D ZVS is compared in fig.91. Both dataset were collected by using optimal DC load condition for each amplifier topology. During the measurement input voltage was increased until DC power supply current limit was reached at 1A. In table 28 are shown main electrical parameters during test.

Table 28 DUTs in fig.91.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
CE	9,00-20,0	0,43-1,03	3,87-20,6	10,2-24,0	0,28-0,67	2,89-16,1	35
CD ZVS	10,0-27,9	0,45-1,03	4,46-28,8	12,0-33,1	0,24-0,65	2,82-21,6	50

Fig.91 points out that Class E beats Class D ZVS in efficiency in whole power range shown in the chart. Remarkable in table 28 is that Class D ZVS is able to reach 35% higher maximum output power level than Class E with same input current available.

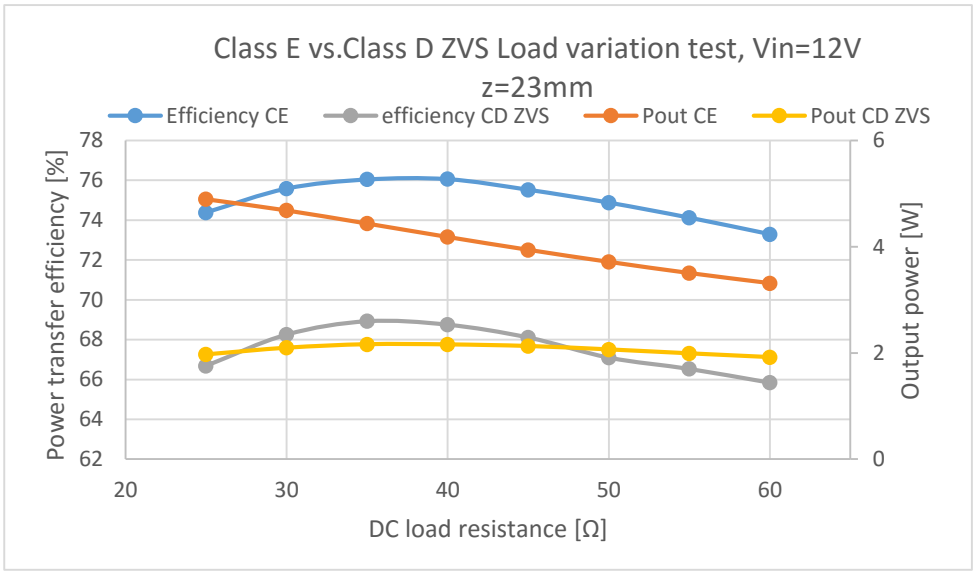

Figure 92 Class E vs. Class D ZVS Load variation test, V_{in}=12V z=23mm

Table 29 DUTs in fig.92.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
CE	12	0,55-0,38	6,58-4,52	11,2-14,3	0,44-0,23	4,89-3,31	25-60
CD ZVS	12	0,24-0,26	2,92-3,14	7,13-10,9	0,28-0,18	1,92-2,16	25-60

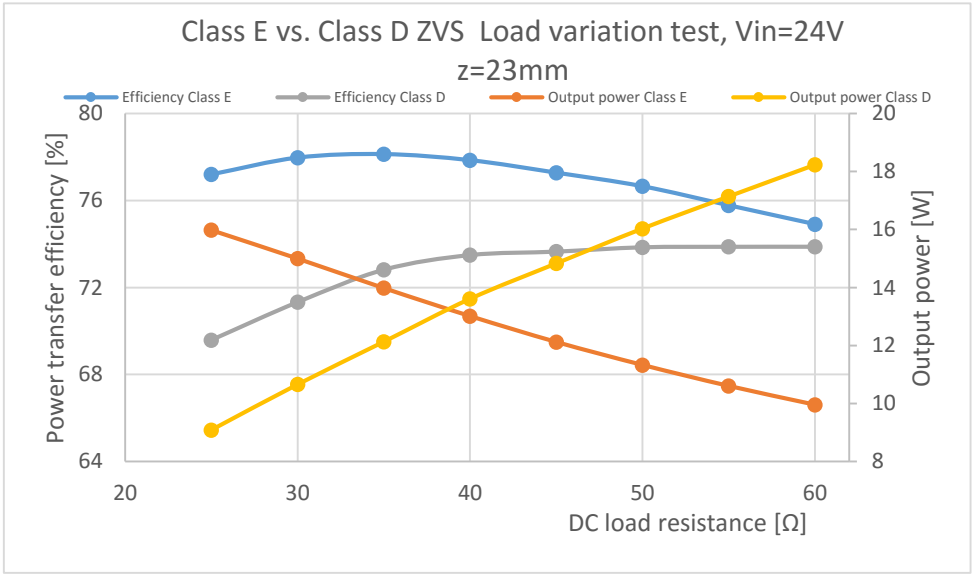

Figure 93 Class E vs. Class D ZVS Load variation test, V_{in}=24V z=23mm

Table 30 DUTs in fig.93.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
CE	24	0,86-0,55	20,7-13,3	20,2-24,7	0,79-0,40	16,0-10,0	25-60
CD ZVS	24	0,54-1,03	13,1-24,7	15,2-33,2	0,60-0,55	9,09-18,2	25-60

The load variation test comparison shown in fig.93 confirms the better power transfer efficiency for Class E, but as we can see increased DC load resistance degenerates more Class E efficiency than Class D ZVS efficiency. Class E sensitivity for load variation is more evident when looking at downward output power delivery curve. Class D ZVS is not as sensitive for DC load variation.

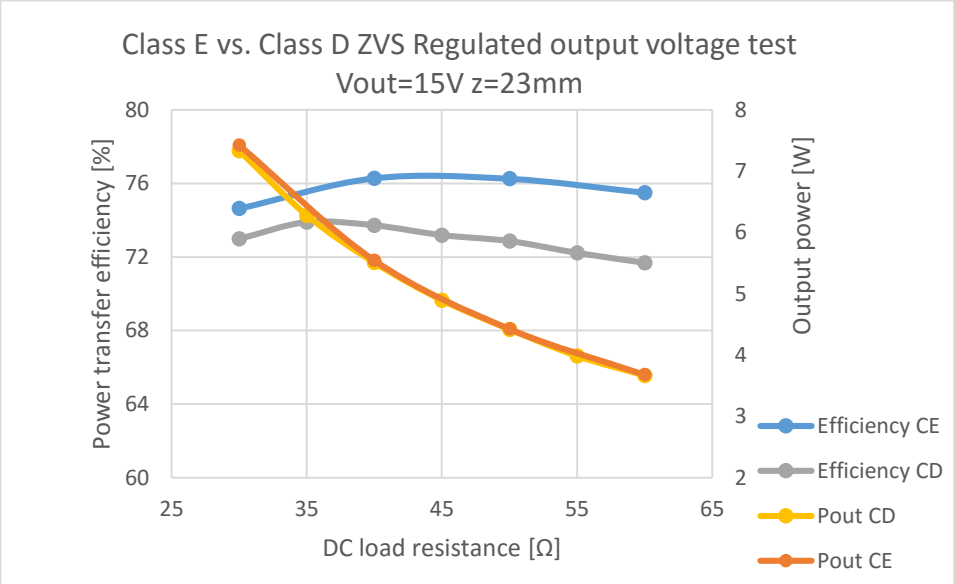

Figure 94 Class E vs. Class D ZVS Regulated output voltage V_{out}=15V z=23mm

Regulated output voltage test comparison make no big difference between topologies under test. Remarkable in fig.94 is almost equal power delivery capability of both amplifier. Both amplifiers suffer from output power delivery declining when DC load resistance is increasing.

Table 31 DUTs in fig.94.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
CE	12,7-10,4	0,78-0,47	9,95-4,88	15	0,50-0,25	7,43-3,68	30-60
CD ZVS	19,8-13,0	0,51-0,40	10,1-5,12	15	0,49-0,24	7,73-3,67	30-60

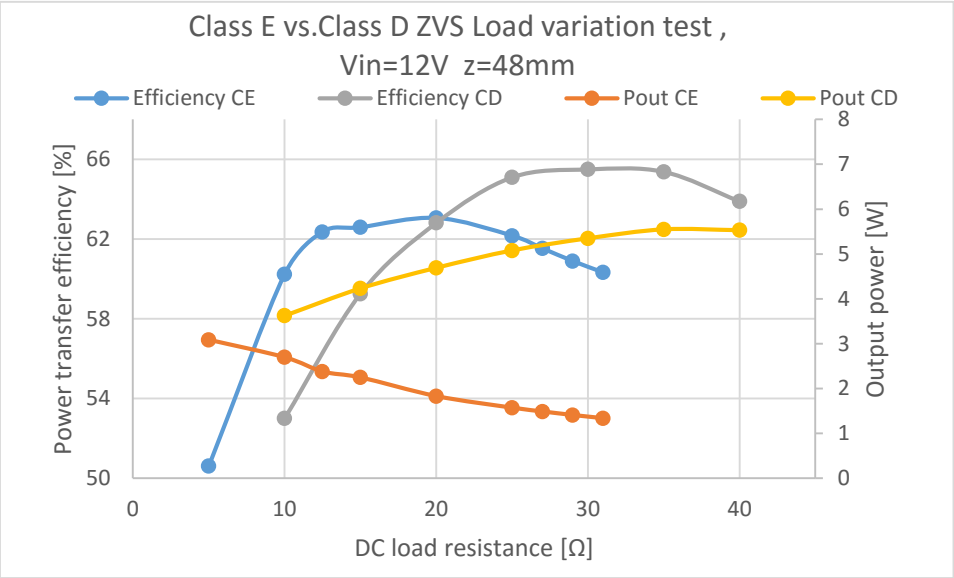

Figure 95 Class E vs. Class D ZVS Load variation test, V_{in}=12V z=48mm

Above fig.95 shows that at in condition where $V_{in} = 12V$ and z=48 Class D ZVS can reach better efficiency. Class D ZVS is operating also well with respect to the output power delivery capability, while DC load resistance increases also output power increases.

Table 32 DUTs in fig.95.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
CE	12	0,51-0,18	6,10-2,22	3,99-6,54	0,78-0,20	3,09-1,34	5,14-32,0
CD ZVS	12	0,57-0,72	6,84-8,65	5,89-15,0	0,62-0,37	3,63-5,53	9,57-40,7

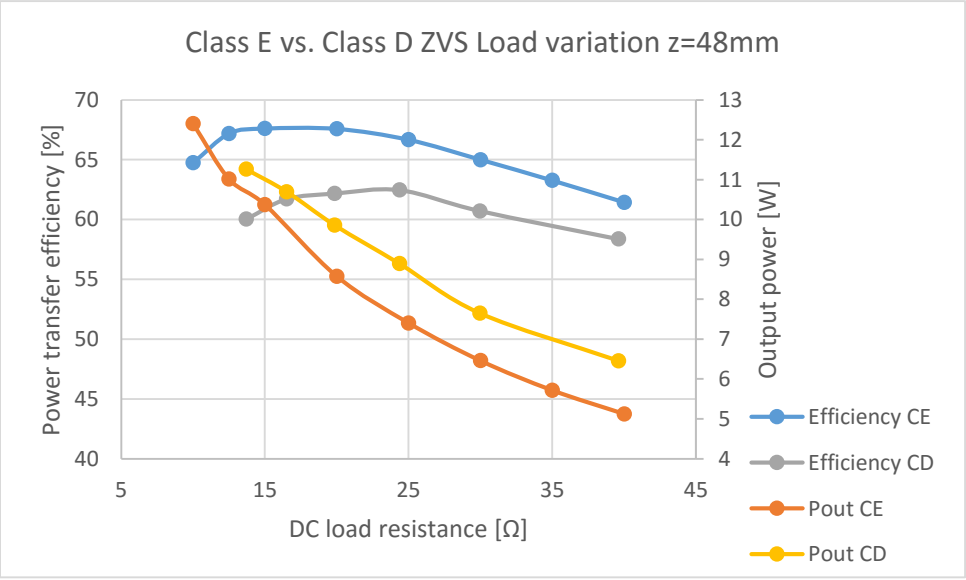

Figure 96 Class E vs. Class D ZVS Load variation z=48mm

Table 33 DUTs in fig.96.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
CE	24	0,80-0,35	19,2-8,34	11,0-14,5	1,12-0,35	12,4-5,12	10-40
CD ZVS	19	0,99-0,58	18,8-11,1	11,4-16,0	0,91-0,40	11,2-6,45	13,7-39,6

At higher supply voltage $V_{in} = 24V$ for Class E and $V_{in} = 19V$ for Class D ZVS. Class E beats Class D ZVS at efficiency. Moreover in fig.96 can be seen how Class D ZVS output power delivery start begins to fall.

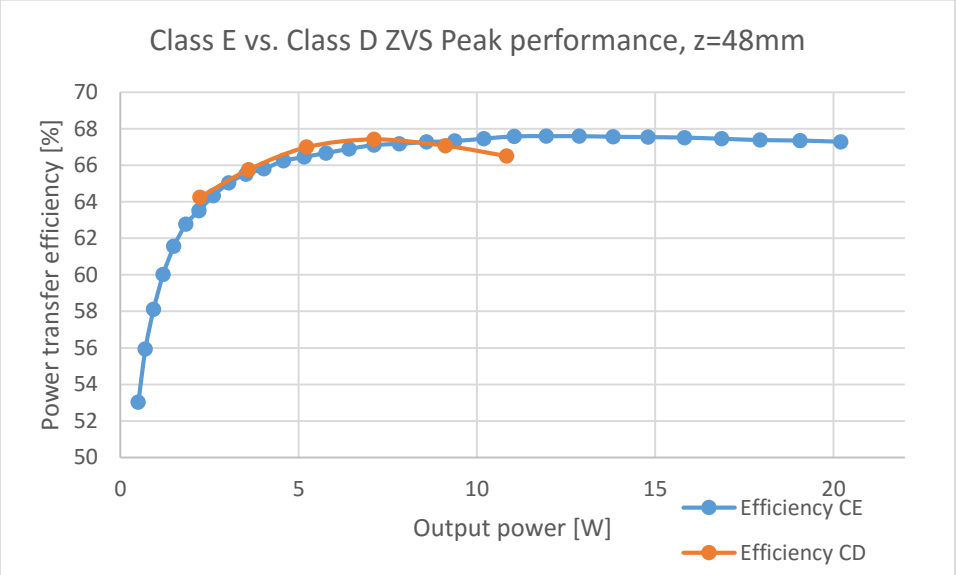

Figure 97 Class E vs. Class D ZVS Peak performance, z=48mm

When observing peak performance of Class E and Class D ZVS in fig.97 figures out that in coil distance of $z = 48mm$ Class D ZVS efficiency crosses the Class E efficiency for first time. DC power supply current limit stopped peak performance test for Class D ZVS and the peak efficiency value was not most probably reached.

Table 34 DUTs in fig.97.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	$R_{DCload}[\Omega]$
CE	8-36	0,16-0,83	1,25-30	3,73-20,1	0,19-1,00	0,70-20,2	20
CD ZVS	8-18	0,47-1,03	3,74-18,6	7,81-18,1	0,30-0,70	2,37-12,7	25

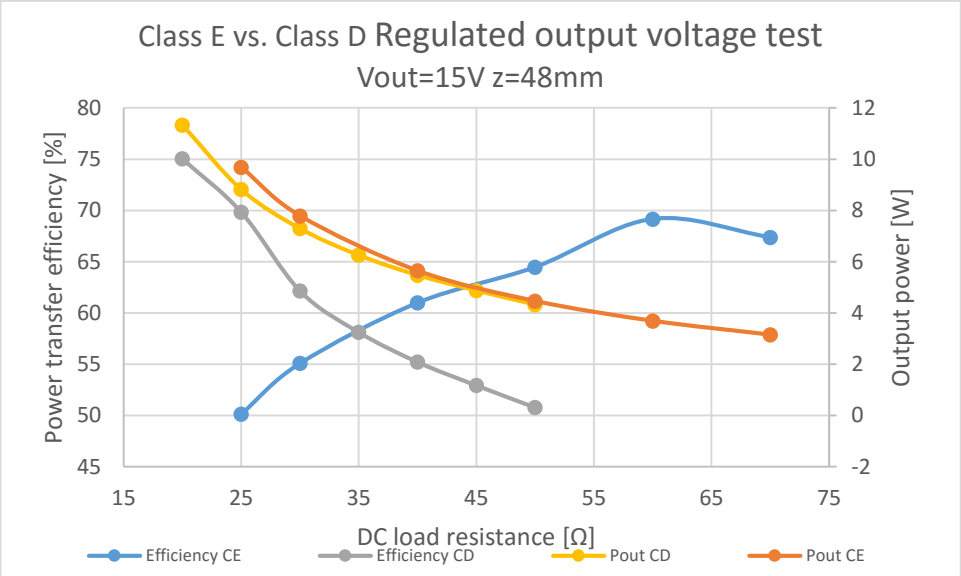

Figure 98 Class E vs. Class D Regulated output voltage test, V_{out}=15V z=48mm

Table 35 DUTs in fig.98.

	Source board			Device board			
	V_{in} [V]	I_{in} [A]	P_{in} [W]	V_{out} [V]	I_{out} [A]	P_{out} [W]	R_{DCload}[Ω]
CE	13,5-6,43	1,44-0,73	19,3-4,68	15	0,65-0,21	9,69-3,15	25-70
CD ZVS	17,7-12,7	1,01-0,57	15,1-8,53	15	0,76-0,29	11,3-4,33	20-50

Regulated output voltage test for Class D ZVS amplifier at $Z = 48mm$ seems to be extremely though. Fig.98 suggest that optimal DC load resistance of Class D ZVS is shifted downwards and optimal DC load resistance of Class E is shifted upwards. Both amplifiers suffer from output power delivery declining.

Topology comparison conclusion

Two amplifier topologies Class E and Class D ZVS was compared on the basis of three different efficiency measurement setup. Peak performance test was carried out by using fixed load resistance and varying supply voltage. During load variation test supply voltage was fixed and for DC load resistance was given different values. Last test performed was the regulated output voltage test where DC output voltage of device coil was fixed and in turn supply voltage and DC load resistance was variables. All measurements were carried out in two different distance between coils $z = 23mm$ and $z = 48mm$.

Topology comparison showed that Class E gives clearly higher efficiency value than Class D ZVS at $z = 23mm$ distance. Also was shown that in this work studied Class E type WPT system is more severe for DC load variations than Class D ZVS. When DC load is increasing Class E can still maintain relatively high efficiency but the output power delivery is decreasing. During the same load variation test Class D ZVS efficiency stayed constant or even slightly improved, characteristic for Class D ZVS is that output power delivery capability increases when DC load resistance is increasing.

This is mainly due to coil set natural characteristics. Output voltage regulation test was very much the same for both amplifier types.
Surprisingly at distance $z = 48mm$ Class D ZVS showed better efficiency counts when operating in 5W power level or above that. Again this can be explained by Class E vulnerability against loading condition variation. It is worth to note that at distance $z = 48mm$ Class E amplifier is able to deliver 60% more power into load than Class D ZVS when same DC power supply is used for both cases. Instead at distance $z = 23mm$ Class D ZVS amplifier is able to deliver 34% more power into load than Class E when utilizing same DC power supply.

Load variation test was accomplished with $V_{in} = 12V$ and $V_{in} = 24V$ supply voltages. According to the measurements it seems that Class D ZVS tends to work better with higher supply voltage and Class E more likely works better with lower supply voltage level at distance z=48mm. Load regulation test at distance z=48mm proved to be challenging for both amplifier types. It is possible that by choosing different regulated output voltage value this test would show less turbulent behaving in measured quantities.

When considering which of the amplifier topologies studied here would be more suitable under certain circumstances or in specific application following attributes should be noticed:

- coil distance
- desired output power level
- efficiency requirement
- applicable supply voltage
- needed load variation range.

At this point coil set features and relevance in different applications is neglected and only amplifier topology related issues are discussed here. In table 36 below is simple topology selection table which is formulated on basis of topology comparison discussion earlier. This table can be used as a guideline when needed to evaluate which topology would be suitable in each design case. When using this topology selection table, first coil distance value is selected. Next designer need to define three design specifications on the row and pick from the table topology that supports the chosen specification. At the end that topology which gather most hits is the right choice for that design case.

Table 36 Topology selection table.

Coil distance	low P_{out}	high P_{out}	wide load range	narrow load range	$V_{supply} = 12V$	$V_{supply} = 24V$
z=23mm	CE	CD ZVS	CD ZVS	CE	CE	CE
z=48mm	CD ZVS	CE	CE(24V)/CD(12V)	CE	CD ZVS	CE

Though, there is used some specific values for z-distance and V_{supply} in the topology selection table, it can still be used for evaluating suitable topology if design specification values are not exactly the same but are the same order of magnitude. In the

following tables 37 – 39 highest efficiency values η_{max} are collected from three different performance tests.

Table 37 Peak performance comparison.

	η_{max} [%] z=23mm	η_{max} [%] z=48mm
Class E	78,50	67,58
Class D ZVS	75,05	67,42

Table 38 Load variation comparison.

	η_{max} [%] z=23mm	η_{max} [%] z=48mm
Class E	76,25	67,38
Class D ZVS	73,72	75,04

Table 39 Regulated output voltage test comparison.

	η_{max} [%] z=23mm	η_{max} [%] z=48mm
Class E	78,14	67,58
Class D ZVS	73,88	62,46

6 Conclusion

The study in this thesis work was set to explore magnetic resonance induction based wireless power transfer in low and medium power applications in context of consumer electronics. Nowadays a person has a large number of different portable devices that need to be charged regularly and most of the people has come up to the challenge in using and storing variety of chargers and cables for different appliances. To ease people frustration and inconvenience wireless power transfer methods has been brought available to consumers. Currently on the market offered wireless chargers are based on tightly coupled electromagnetic induction and they can merely be used to charge one device at a time. The expectations regarded to magnetic resonance induction based wireless power transfer are high because its loose coupling characteristics makes it possible to have chargers that simultaneously can deliver power for multiple devices and with increased positional freedom compared to tightly coupled inductive approaches.

The starting point in this thesis work was to disclose the physical phenomenon behind electromagnetic induction and expand awareness of the exploitation of magnetic resonance induction in wireless power transfer. The system of two coupled coils forms an energy transfer path in magnetic field energy exploiting wireless power transfer. In this work starting from equivalent circuit of coupled LC-resonators it is shown that power can be transferred between loosely coupled source and receiver coils with high efficiency if high Q-value requirement for resonators is fulfilled. Even with coupling factor value $k < 0.1$ can such resonator coils be realized that are able to deliver power in higher than 90% coil-to-coil efficiency. Wireless power transfer system figure-of-merit with respect of resonator individual Q-values (Q_S , Q_D) and coupling factor k was found to be:

$$FOM_{WPT} = k\sqrt{Q_S Q_D} \ .$$

Current standard proposal in area of magnetic resonance induction based wireless power transfer has chosen the operating frequency of 6.78MHz. That frequency is somewhat higher than typically seen in switch mode power electronics and it sets requirements for the power amplifier in the system as high efficiency is essential. In this work studied Class E and Class D ZVS amplifiers both showed their capability to deliver power with high efficiency in wireless power transfer system. The efficiency were measured as DC power received in load divided by DC power supplied into amplifier. This measurement arrangement included rectifier losses in receiver side but amplifier driving circuit losses were excluded. Table 40 below shows the maximum efficiency values achieved in two different distance z between coils.

Table 40 Maximum efficiencies of Class E and Class D ZVS.

Topology	η_{max} [%] $z = 23mm$	η_{max} [%] $z = 48mm$
Class E	78,50	67,58
Class D ZVS	75,05	67,42

As both amplifiers are in principle zero voltage switching topologies, there are tuning issues that can influence the reliability of measurement results. Comparing the two amplifier performance is difficult if both amplifiers are not optimally tuned. As Class E tends to be more vulnerable to load variation Class D ZVS efficiency is more related to

optimal dead-time adjustment. However both amplifier were tuned as precisely as possible before measurements and same source and receiver coil set was used. In Class E is very attractive that it utilizes only one switching device while Class D ZVS need those two and in addition more complicated driver circuit. It is possible that Class D ZVS lower efficiency is due to two switching device and theoretically twice as high switching losses.

The higher operation frequency sets requirements also for the switching devises. Fast switching times are needed or soft switching techniques need to be utilized to avoid oversized switching losses in power transistor. New challenger for traditional Si MOSFET is GaN FET which are spreading from radio engineering to the power electronics. GaN FETs extremely small parasitic capacitances and inductances makes them interesting alternative for MOSFET in wireless power transfer. Though GaN FET were used in this work in ZVS topology it is possible to use them in hard switching topology power amplifier even with decent switching losses. While MOSFET parasitic properties are the determinant factor in circuit design whereas with GaN FET it is more question of careful layout design. So far the price per unit for GaN FET is much higher than MOSFET and the suitability for mass production is questionable. Even though GaN FET have superior characteristics compared to MOSFET, it is perhaps too early to forget silicon MOSFETs. At least in Class D ZVS were switching voltage waveform rise time is slowed down remarkably GaN FET excellent fast switching properties are not fully exploited and sufficient MOSFET for more affordable price could be better option. As source coils are relatively large in magnetic resonance induction WPT, the industrial design cannot be very tightly outfitted and there is also plenty room for electronics, then the larger outline of MOSFET does not matter.

For sure EMI issues are big challenge in magnetic resonance induction WPT system. High switching frequency, high current and fast switching transitions are liable to constitute challenging EMI issues. As operation frequency is fixed according to magnetic resonance induction specification and current is needed to transfer power the remaining option is to slow down switching transitions. In that case ZVS operating amplifier topologies are ideal as they shapes voltage waveforms from square to more trapezoidal form. During this work Fourier-series envelope curve for trapezoidal waveform was used to prove the fact that slowing down square wave rising and falling edges have great impact in reducing harmonic components. Increasing rise time from 1ns to 15ns reduces troublesome harmonic frequency bandwidth more than one decade. Unfortunately this work do not give thorough solution how to pass official EMC test practices, but it offers some guidance and knowledge of critical EMI issues in design and PWB layout.

One technical challenge that is touched only briefly in this work is adaptive matching between amplifier and coil set. In proposal for magnetic resonance induction standard there is defined complex impedance range that power amplifier need to be able drive, yet at a certain defined efficiency level. This reflected impedance range is defined in the frame that loading of WPT system varies as one or more appliances are charged at same time and how the appliances are positioned over source coil and how loading is varying during the battery charging cycle. In practice tuning the matching would be implemented by adding capacitors that can be switched in or out from the circuit. For sure there have to be function that detects amplifier operation condition, makes decision if impedance need to be changed and some actuator that switch capacitors on or off. Later studies will be needed how adaptive matching is implemented. Amplifier topology that have narrow impedance capability range needs more complicated and expensive matching functions to meet standard requirements than amplifier topology

with wider impedance driving capability range. On the basis of this thesis Class D ZVS amplifier seems to have wider impedance driving capability range compared to Class E.

In order to increase consumer convenience with portable electrical devices this thesis work introduced magnetic resonance induction based wireless power transfer as a solution. Several challenges related to topic were discussed and some practical tools to help further research and development were founded. The following years will show if high expectations loaded into magnetic resonance induction push its way to success.

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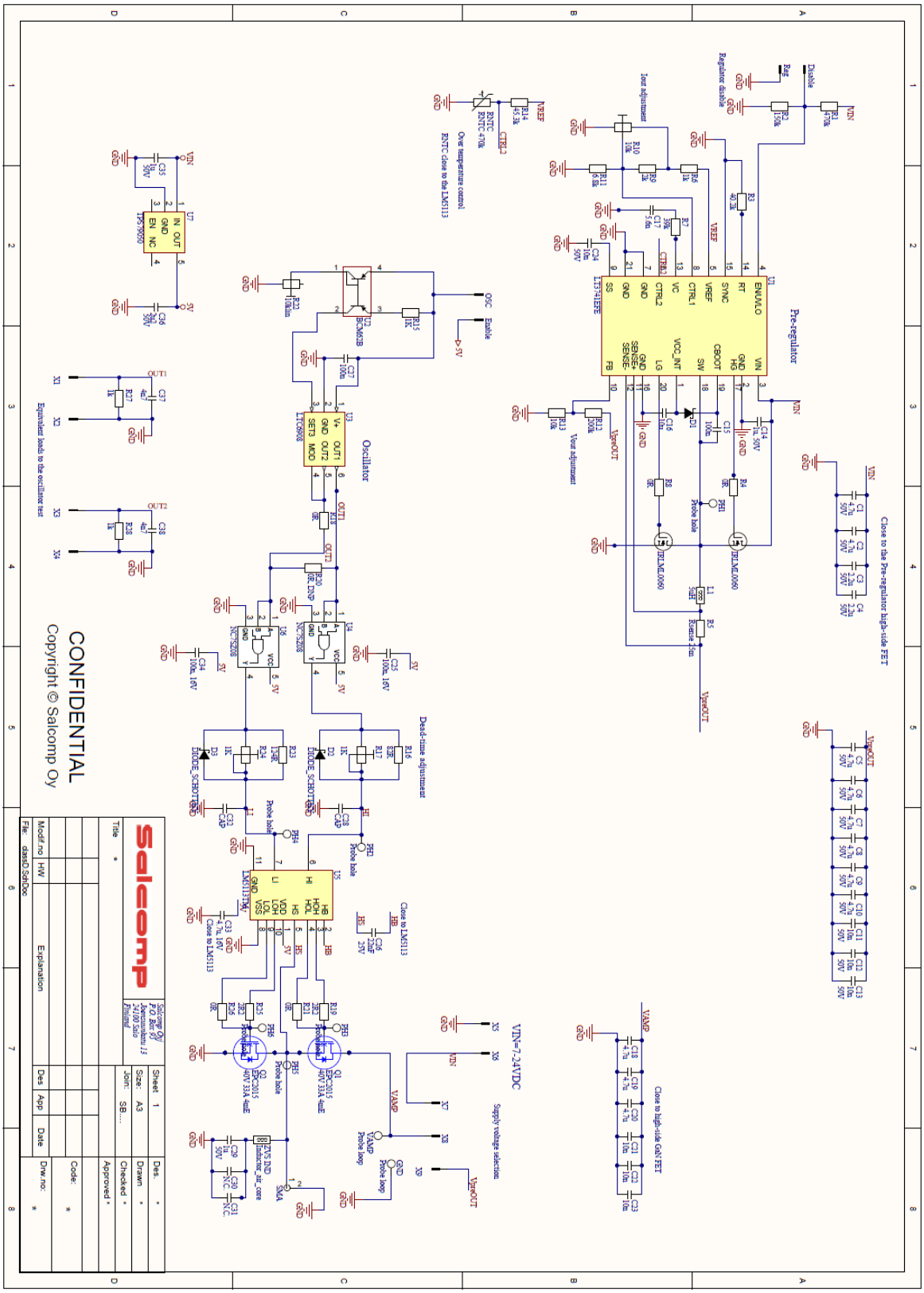
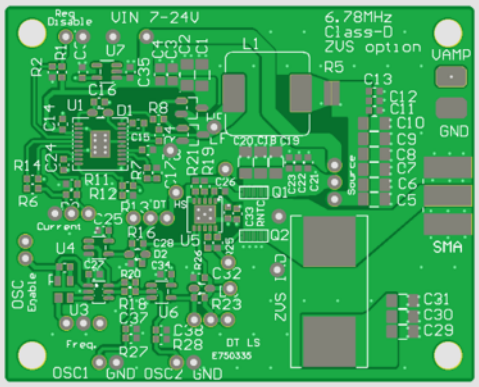
Appendix

A Class D ZVS circuit schematic

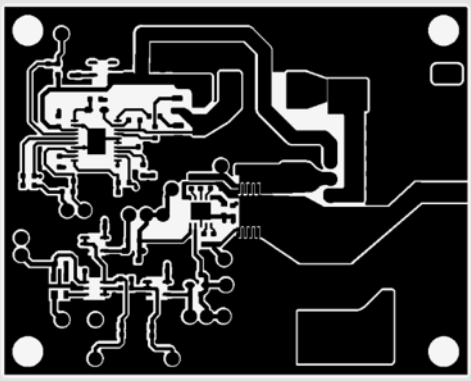


B Class D ZVS PWB layout

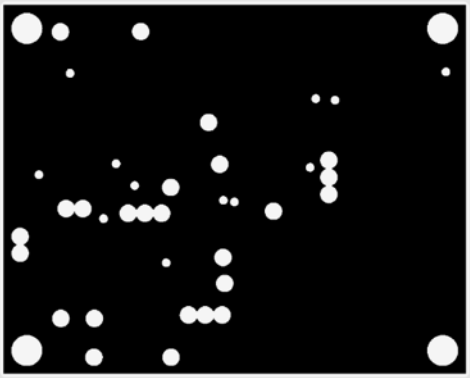
E750335 PCB view TOP (topview)



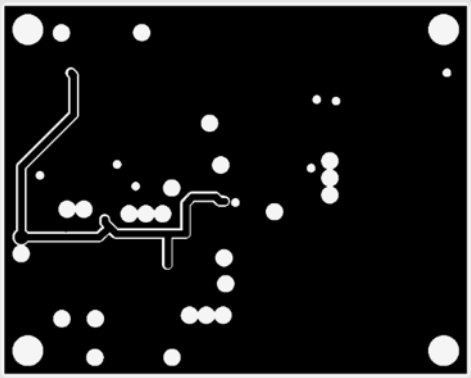
E750335 TOP layer Image (topview)



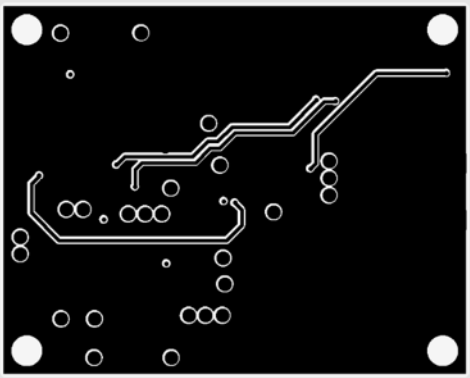
E750335 Innerlayer 2 Image (topview)



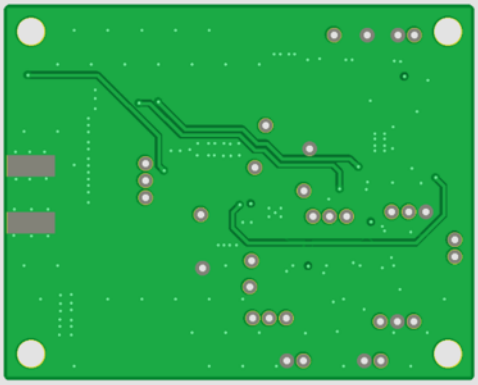
E750335 Innerlayer 3 Image (topview)



E750335 BOTTOM layer Image (topview)



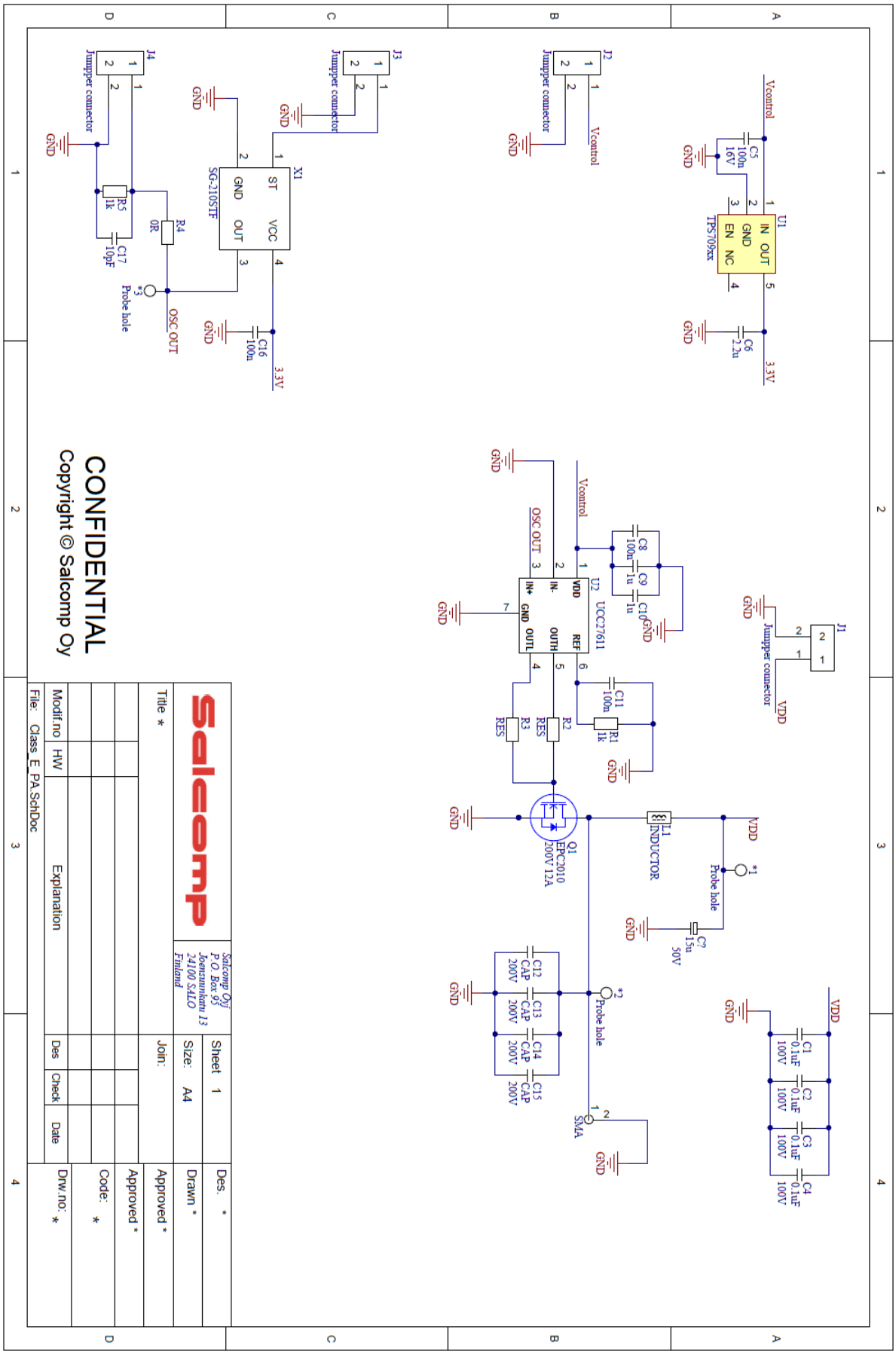
E750335 PCB view BOTTOM (bottomview)



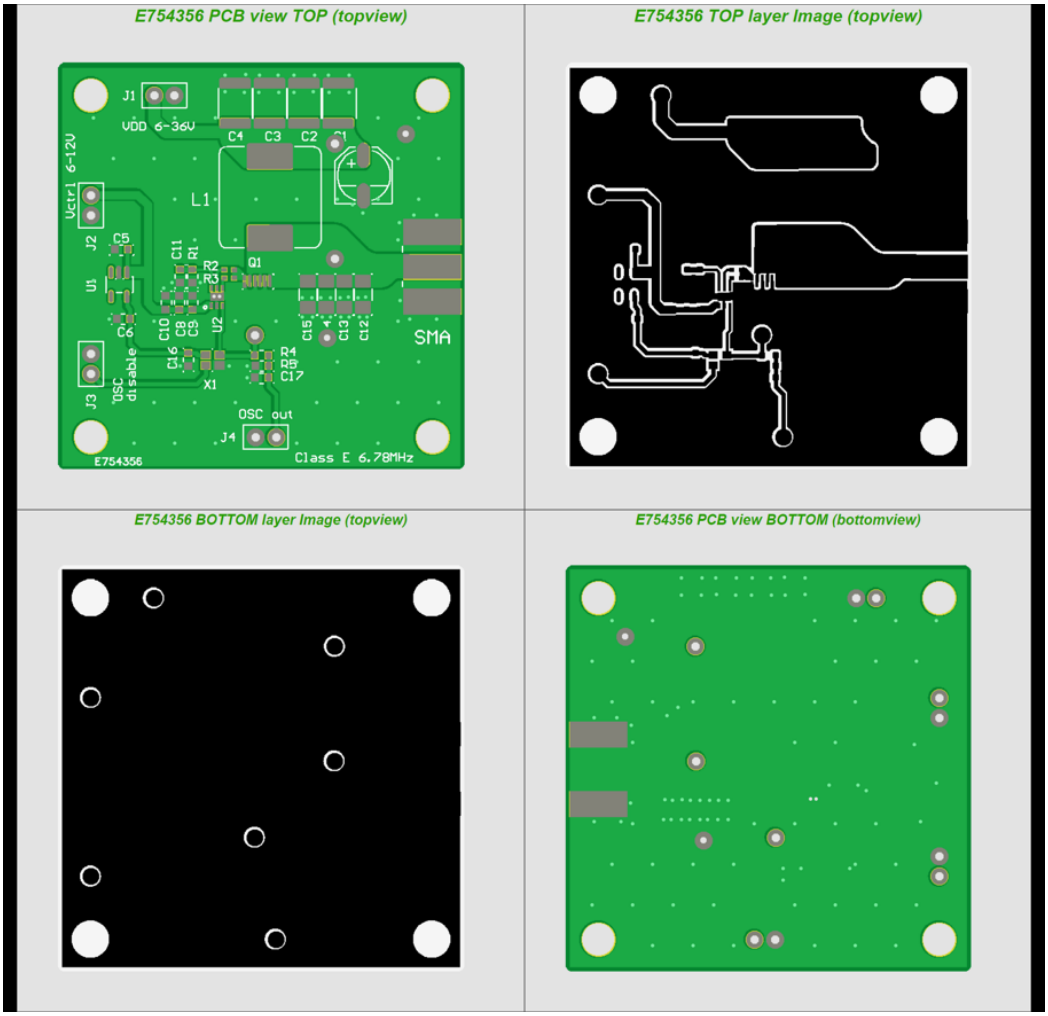
C Class D ZVS BOM					
Comment	Description	Designator	Footprint	LibRef	Quantity
4.7u	CCA 4u7 10% 50V X7R 1206	C1, C2, C5, C6, C7, C8, C9, C10, C18, C19, C20	1206R_R	CAP	11
2.2u	CCA 2u2 20% 50V X7R 0805	C3, C4	0805R_C	CAP	2
10n	CCA 10n 20% 50V X7R 0603	C11, C12, C13, C21, C22, C23, C24	0603R_R	CAP	7
1u, 50V	CCA 1u 10% 50V X7R 0603	C14	0603R_R	CAP	1
100n	CCA 100n 10% 50V X7R 0603 , CCA 100n 10% 16V X7R 0603	C15, C27	0603R_R	CAP	2
10u	CCA 10uF 20% 25V X5R 0603	C16	0603R_R	CAP	1
5.6n	CCA 5n6 10% 50V X7R 0603	C17	0603R_R	CAP	1
100n, 16V	CCA 100n 10% 16V X7R 0603	C25, C34	0603R_R	CAP	2
22nF	CCA 22n 10% 25V X7R 0603	C26	0603R_R	CAP	1
CAP	CCA 47p 5% 50V NP0 0603	C28, C32	0603R_R	CAP	2
1u	CCA 1u 10% 50V X7R 0805	C29, C35	0805R_SS	CAP	2
N.C.	CCA 1u 10% 50V X7R 0805	C30, C31	0805R_SS	CAP	2
4.7u, 16V	CCA 4u7 10% 16V X5R 0603	C33	0603R_R	CAP	1
2u2	CCA 2u2 10% 50V X7R 0805	C36	0805R_SS	CAP	1
4n7	CCA 4n7 10% 10V X7R 0402	C37, C38	0603R_R	CAP	2
DIODE_SCHOTTKY	NXP 1PS79SB40 Small Signal Schottky Diode, Single, 40 V, 120 mA	D1, D2, D3	SOD-110	DIODE_SCHOTTKY	3
DC-CONNECTOR_1	DC-Connector_1	Disable, Enable, OSC, X1, X2, X3, X4, X5, X6, X7, X8, X9	DC-con_1	DC-CONNECTOR_1	13
Probe loop	TEST POINT, SMT	GND, VAMP	Probe loop	Probe loop	2
IRLML0060	MOSFET, N CH, 60V, 2.7A, SOT-23	HF, LF	sot-23	IRLML0060TRPBF	2
5uH	Inductor, 5uH, 20%, 4.7A, SMD	L1	Inductor_SMD_12.5*12.5	INDUCTOR	1
Probe hole	TEST POINT	PH1, PH2, PH3, PH4, PH5, PH6	DC-con_1	Probe hole	6
EPC2015	GaNFET, EPC2015 40V 33A 0.004R	Q1, Q2	EPC2x40L	EPC2015	2
470k	CRES 0W10 470K F 0603	R1	0603R_R	RES	1
150k	CRES 0W10 470K F 0603	R2	0603R_R	RES	1
40.2k	CRES 0W10 40K2 D 0603	R3	0603R_R	RES	1
0R	CRES 0W10 0R D 0603	R4, R8, R18, R21, R26	0603R_R	RES	5
Rsense 25m	SMD Current Sense Resistors, FC4L Series, 0.025 ohm, 1 W, ± 1%, 1206 Wide	R5	1206R_R_wide	RES	1
1k	CRES 0W10 1K J 0603	R6, R15, R27, R28	0603R_R	RES	4
39k	CRES 0W10 39K J 0603	R7	0603R_R	RES	1
2k	CRES 0W10 2K J 0603	R9	0603R_R	RES	1
10k	TRIMMER, POT, 10K, 23 Turn, THD	R10	Trimmer_R2.5_line	RES_TRIM	1
6.8k	CRES 0W10 6K8 F 0603	R11	0603R_R	RES	1
200k	CRES 0W10 200K D 0603	R12	0603R_R	RES	1
10k	CRES 0W10 10K D 0603	R13	0603R_R	RES	1
45.3k	CRES 0W10 45K3 D 0603	R14	0603R_R	RES	1
82R	CRES 0W10 82R D 0603	R16	0603R_R	RES	1
1K	TRIMMER, POT, 1K, 23 Turn, THD	R17, R24	Trimmer_R2.5_line	RES_TRIM	2
2R2	CRES 0W10 2R2 D 0603	R19, R25	0603R_R	RES	2
0R, DNP	CRES 0W10 0R D 0603	R20	0603R_R	RES	1
10klin	TRIMMER, POT, 10K, 23 Turn, THD	R22	Trimmer_R2.5_line	RES_TRIM	1
124R	CRES 0W10 124R D 0603	R23	0603R_R	RES	1
RNTC 470k	NTC-RES 470k 0603 B4100	RNTC	0603R_R	RES_NTC	1
SMA_CON	CONN,SMA_Connector	SMA	SMA Edge Connector	SMA_CONNECTOR	1

LT3741EFE	LT3741EFE, DC/DC CONTROLLER, BUCK, 1MHz	U1	TSSOP-20	LT3741EFE	1
BCM62B	Transistor, PNP/PNP Matched, SOT143B	U2	SOT-143	BCM62B	1
LTC6908	OSCILLATOR, COMP O/P, SMD, TSOT236	U3	SOT-23-6	LTC6908	1
NC7SZ08	AND Gate, NC7SZ08	U4, U6	SOT-23-5	NC7SZ08	2
LM5113TM	LM5113SD/NOPB	U5	WSON-10	LM5113TM	1
TPS79050	TPS70950DBVT LDO, 5V, 0.15A	U7	SOT-23-5	TPS790xx	1
Ind aircore	Inductor AIR CORE	ZVS IND	Ind aircore	Ind aircore	1

D Class E circuit schematic



E Class E PWB layout



F Class E BOM

Comment	Description	Designator	Footprint	LibRef	Quantity
Probe hole		P1, P2, P3	DC-con_1	Probe hole	3
0.1uF	CCA 100n 5% 100V X7R 1812	C1, C2, C3, C4	1812R	CAP	4
100n	CCA 100n 10% 16V 0603	C5, C8, C11, C16	0603R_R	CAP	4
2.2u	X5R or X7R	C6	0603R_R	CAP	1
1u	CCA 1u 10% 16V 0603	C9, C10	0603R_R	CAP	2
CAP	CCA 2% C0G 200V High Q	C12, C13, C14, C15	1206R_C	CAP	4
10pF	CCA 10p 10% 16V 0603	C17	0603R_R	CAP	1
15u	Electrolyte Capacitor SMD	C?	SMD_ELCAP_6.5	CAP_EL	1
Jumpper connector		J1, J2, J3, J4	Connector 2-pin	Jumpper connector	4
INDUCTOR	Inductor 68uH, 20%, 3.2A	L1	Inductor_SMD_12.5*12.5	INDUCTOR	1
EPC2010	GaNFET, EPC2010 200V 12A 25mE	Q1	EPC2x200L	EPC2010	1
1k	CRES 0W10 1K 0603	R1, R5	0603R_R	RES	2
RES	CRES 0W10 0R 0603	R2, R3	0402R	RES	2
0R	CRES 0W10 0R 0603	R4	0603R_R	RES	1
SMA_CON	CONN,SMA_Connector	SMA	SMA Edge Connector	SMA_CONNECTOR	1
TPS709xx	LDO	U1	SOT-23-5	TPS709xx	1
UCC27611	GaN FET driver	U2	SON-6_EPAD	UCC27611	1
SG-210STF	Oscillator	X1	Osc xo	SG-210STF	1